VT1434A

4-Channel 65 kSamples/s Arbitrary Source

User's Guide

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In This Book

The VT1434A 4-Channel 65 kSamples/s Arbitrary Source is a C-sized VXI module. "65 kSamples/s" refers to the maximum signal data rate of 65,536 samples per second. The VT1434A may contain one or two 2-channel source assemblies so that the module may have a total of up to four outputs. In addition, if option 1D4 is installed, it provides one additional output for a total of five output channels. The module plugs into a single, C-size slot in a VXI mainframe.

This book documents the VT1434A module, including information on how to use it. It provides:

- Descriptions of the module and its measurement process
- Description of the 1D4 additional Arbitrary Source option
- Details about the module's VXI registers
- A summary of the Host Interface Library which can be used to control the module, including VXI*plug&play* libraries.
- Instructions for printing the Function Reference for the Host Interface Library if desired. The Function Reference can be accessed by way of online manual pages.

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Support Resources

Support resources for this product are available on the Internet and at VXI Technology customer support centers.

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1

Installing the VT1434A

Installing the VT1434A

This chapter contains instructions for installing the VT1434A 4-Channel 65 kSamples/s Arbitrary Source Module and its drivers. This chapter also includes instructions for transporting and storing the module.

To inspect the VT1434A

The VT1434A 4-Channel 65 kSamples/s Arbitrary Source Module was carefully inspected both mechanically and electrically before shipment. It should be free of marks or scratches and it should meet its published specifications upon receipt.

If the module was damaged in transit, do the following:

- Save all packing materials.
- File a claim with the carrier.
- Call a VXI Technology sales and service office.

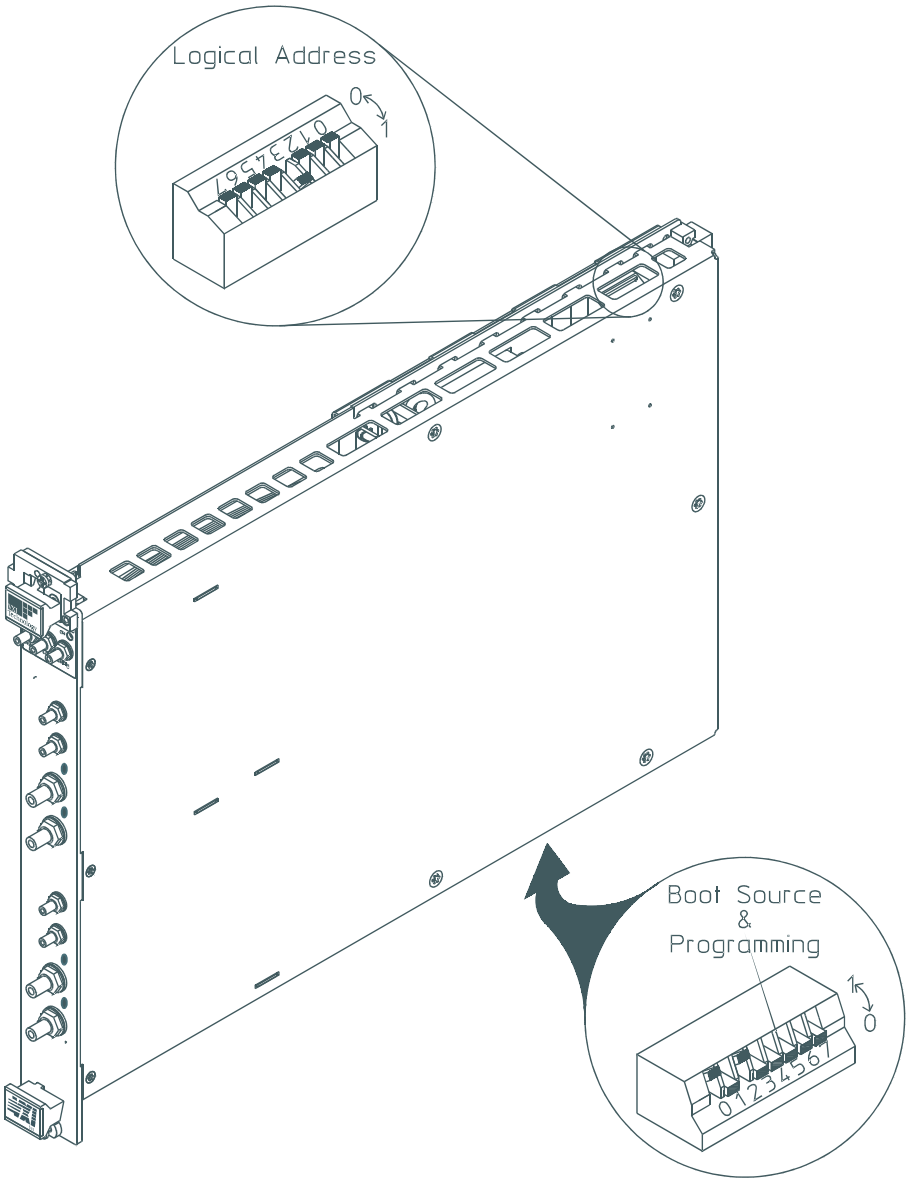
To install the VT1434A

Caution To protect circuits from static discharge, observe anti-static techniques whenever handling the VT1434A 4-Channel 65 kSamples/s Arbitrary Source Module.

1. Set up the VXI mainframe. See the mainframe's installation guide.
2. Select a slot in the VXI mainframe for the VT1434A module.
   Unlike some VXI modules, it is not critical to place a VT1434A module immediately to the left or right of another module for use of the Local Bus. If the VT1434A has a Local Bus option, it is used only to pass data from the module on the left to the module on the right. The VT1434A does not use or modify the Local Bus data.
3. Using a small screwdriver or similar tool, set the logical address configuration switch on the VT1434A.
   (See the illustration on the next page.) Each module in the system must have a unique logical address. The factory default setting is 0000 1000 (8). If a GPIB command module will be controlling the VT1433B module, select an address that is a multiple of eight. If the VXI system dynamically configures logical addresses, set the switch to 255.

4 Check the settings of the Boot Source and ROM Programming switches on the bottom of the module.

Set switches 1 and 3 (BS1 and BS3) up and all the other switches down.



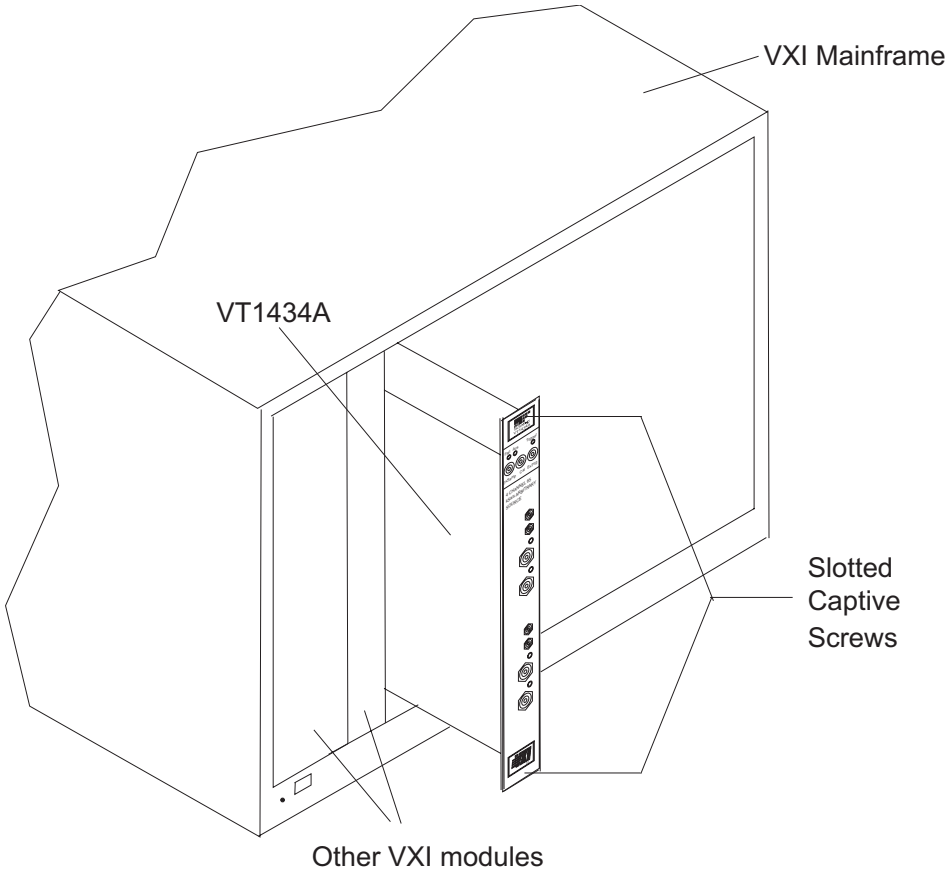
Caution Installing or removing the module with power on may damage components in the module.

5 Set the mainframe's power switch to standby (⏻).

6 Place the module's card edges (top and bottom) into the module guides in the slot.

7 Slide the module into the mainframe until the module connects firmly with the backplane connectors. Make sure the module slides in straight.

8 Attach the module's front panel to the mainframe chassis using the module's captive mounting screws.



Install the host interface libraries

The VT1434A is supported by the VT1432A distribution which is supplied with the VT1434A. See the chapter “Getting Started with the VT1434A” for information on installing the software.

To store the module

Store the module in a clean, dry and static free environment.

For other requirements, see storage and transport restrictions in the chapter titled: "Specifications."

To transport the module

Package the module using the original factory packaging or packaging identical to the factory packaging.
Containers and materials identical to those used in factory packaging are available through VXI Technology.

If returning the module to VXI Technology for service, attach a tag describing the following:

- ❑ Type of service required
- ❑ Return address
- ❑ Model number
- ❑ Full serial number

In any correspondence, refer to the module by model number and full serial number.

Mark the container FRAGILE to ensure careful handling.

If necessary to package the module in a container other than original packaging, observe the following (use of other packaging is not recommended):

- ❑ Wrap the module in heavy paper or anti-static plastic.
- ❑ Protect the front panel with cardboard.
- ❑ Use a double-wall carton made of at least 350-pound test material.
- ❑ Cushion the module to prevent damage.

Caution

Do not use styrene pellets in any shape as packing material for the module. The pellets do not adequately cushion the module and do not prevent the module from shifting in the carton. In addition, the pellets create static electricity which can damage electronic components.

2

Getting Started With the VT1434A

Introduction

This chapter shows how to install the software libraries for the VT1434A.

For more information see the other chapters in this book and the on-line function reference. (See “Where to get more information” in the chapter titled “Using the VT1434A").

Two versions of the Host Interface Library are available. One is HP-UX C-Language Host Interface Library which uses SICL (the Standard Instrument Interface Library) to communicate to the VT1433B hardware. The other is the HP-UX, Windows 95 or later and Windows NT VXI*plug&play* Library which communicates with the hardware using VISA (Virtual Instrument Software Architecture.) VISA is the input/output standard upon which all the VXI*plug&play* software components are based.

The VXI*plug&play* Library is compatible with the HP-UX, Windows 95 or later and Windows NT and communicates with the hardware using VISA (Virtual Instrument Software Architecture). VISA is the input/output standard upon which all the VXI*plug&play* software components are based.

This chapter mainly covers the VXI*plug&play* version and it also includes some examples using the C-Language version. If using the C-Language version, refer to the chapter titled "The Host Interface Library" as well.

NOTE

The C-Language Host Interface Library has been provided for the purpose of backward compatibility and is no longer supported. New users should use the VXI*plug&play* Library while older users are encouraged to migrate their applications to the VXI*plug&play* library.

To install the VXI*plug&play* libraries

System Requirements (Microsoft Windows and NT)

An IBM compatible personal computer with either Microsoft Windows 95 or Microsoft Windows NT. (With either Windows 95 or later or Windows NT, use the VXI*plug&play* library).

Additional hardware and software to connect the IBM compatible computer to a VXI mainframe.

Software is supplied on CD-ROM.

System Requirements (HP-UX 10.20)

One of the following workstations:

- An HP V743 VXI-embedded workstation.
- A stand-alone HP Series 700 workstation with an Agilent/HP E1489I EISA-to-MXIbus card and an Agilent/HP E1482B VXI-MXI Bus Extender.

Software is supplied on CD-ROM, so a CD-ROM drive is needed.

HP-UX Version 10.20. This version of HP-UX can use either the C-Language library or the VXI*plug&play* library.

SICL/VISA (Agilent/HP product number E2091E, version E.01.01 or later).

VT1432A Software Distribution

The VT1432A distribution (software) is shipped on a CD-ROM with the VT1434A module. This software works with the VT1432A, VT1433B and VT1434A modules. This distribution includes the VT1432A C-Language Host Interface Library for HP-UX, the VT1432A VXI*plug&play* Host Interface library for HP-UX, Windows 95 or later and Windows NT with associated examples and manual pages.

Getting Updates (Windows)

The latest version of the VT1433B instrument drivers can be found on-line at www.vxitech.com.

Getting Updates (HP-UX)

For the latest HP-UX instrument drivers, please contact VXI Technology Customer Support Services. Contact information can be found in the *Need Assistance?* section at the end of the manual.

To install the Windows VXI*plug&play* drivers for the VT1432A (for Windows 95 or later and Windows NT)

1 Insert the VXI*plug&play* Drivers and Product Manuals CD into the CD-ROM drive.

2 Run the program: d:\drivers\DAQ Drivers\driver_vxipnp_e1432_a_06_13.exe. (If the disc is in a driver other than "drive d:," replace "d:\" with the letter of the drive containing the driver disc.) Note that the driver for the VT1434A are the same as the driver used by the VT1432A. Also note that the "a_06_13" references the software revision and will vary. Follow the on-screen instructions to continue.

3 The *VISA Installation Information* dialogue box will appear. This indicates window will indicate whether or not the VISA library has been correctly installed previously. If not installed, an error message will appear as a reminder to install the library. Click Next to continue.

4 The *Choose Program Folder Items* dialogue box provides options that can be included in the Start Menu Program Folder for the VT1432A. Press Next when finished with selections to continue.

5 The *Select Program Folder* dialogue box appears providing the opportunity to change the name of the program folder that will be created in the Start Menu. The default name is "VXIPNP." Click Next to continue.

6 Setup creates a program group called “Hpe1432” (located typically in c:\VXIPNP\WINNT). It includes:

An icon to run the Soft Front Panel
An icon for HELP text
An icon for UNISTALL the README text can be included optionally.

These icons can also appear in the Startup Menu Program Files (see step 6).

7 After the program files load, the *Setup Complete* dialogue box will appear. It provides the opportunity to view the Readme file and to run the Soft Front Panel upon completion of set up. Click Next after the desired selections are made.

To install the HP-UX VXI*plug&play* drivers for the VT1434A (for HP-UX systems)

1 Log in as root.

2 Insert the VT1432A CD-ROM into the CD-ROM drive or obtain the latest VT1432A distribution.

3 Type `swinstall`.

See the HP-UX Reference manual for information on the swinstall command.

The VT1432A distribution is usually installed in the /opt/vxipnp/hpux/hpe1432/ directory. The files have extensions such as .h, .fp, .sl and .hlp.

The Resource Manager

The Resource Manager is a program from the hardware interface manufacturer. It looks at the VXI mainframe to determine what modules are installed. It is necessary to run it every time the mainframe is powered up. If a message "No VT1434A can be found in this system" message is received, run the Resource Manager.

Before running the VT1432A software make sure that the hardware is configured correctly and that the Resource Manager runs successfully. Before using the the measurement system, all of its devices must be set up, including setting their addresses and local bus locations. No two devices can have the same address. Usually addresses 0 and 1 are taken by the Resource Manager and are not available.

For more information about the Resource Manager, see the documentation provided with the hardware interface.

3

Using the VT1434A

Introduction

This chapter shows how to use the VT1434A using the VXI*plug&play* Host Interface Library.

The VT1434A uses the same software as the VT1432A 16 Channel 51.2 kSamples/s Digitizer plus DSP.

The Host Interface Library for the VT1434A is a set of functions that allow the user to program the register-based VT1434A at a higher level than register reads and writes. The library allows groups of VT1434As to be set up and programmed as if they were one entity.

Two versions of the Host Interface Library are included. One is the HP-UX C-Language Host Interface Library which uses SICL (the Standard Instrument Interface Library) to communicate to the VT1433B hardware. It works for HP-UX 10.20. The other is the VXI*plug&play* Library for Windows 95 or later, Windows NT and HP-UX 10.20 which communicates with the hardware using VISA. VISA is the input/output standard upon which all the VXI*plug&play* software components are based.

This chapter covers the VXI*plug&play* version, but it will also be useful to users of the C-Language version. If using the C-Language version, refer to the chapter titled "The Host Interface Library" as well.

The library includes routines to set up and query parameters, start and stop measurements, read and write data and control interrupts. Routines to aid debugging and perform low-level I/O are also included.

For information on diagnostics see the chapter titled “Troubleshooting the VT1434A.”

What is VXI*plug&play*?

VXI Technology uses VXI*plug&play* technology in the VT1434A. This section outlines some of the details of VXI*plug&play* technology.

Overview

The fundamental idea behind VXI*plug&play* is to provide VXI users with a level of standardization across different vendors well beyond what the VXI standard specifications spell out. The VXI*plug&play* Alliance specifies a set of core technologies centering on a standard instrument driver technology.

VXI Technology offers VXI*plug&play* drivers for VEE-Windows. The VXI*plug&play* instrument drivers exist relative to so-called “frameworks”. A framework defines the environment in which a VXI*plug&play* driver can operate. The VT1434A has VXI*plug&play* drivers for the following frameworks: Windows 95 or later, Windows NT and HP-UX.

VXI*plug&play* drivers

The VT1434A uses the same drivers as the VT1432A 16 Channel 51.2 kSamples/s Digitizer plus DSP.

The VT1432A VXI*plug&play* driver is based on the following architecture:

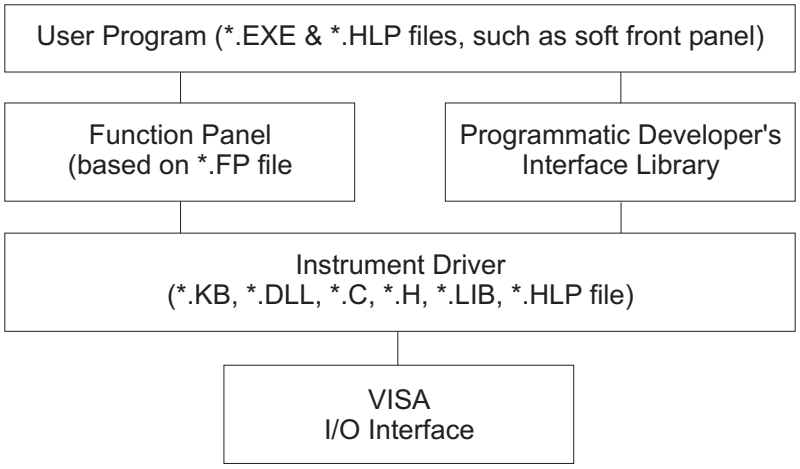


Figure 3-1: VXI*plug&play* driver architecture

It is most useful to discuss this architecture from the bottom up.

The VISA/VTL I/O interface allows interoperability of the VXI*plug&play* driver technology across interfaces.

The actual instrument driver itself is a DLL (Dynamic Linked Library) created from:

- A set of source (.C) files.
- A set of header (.H) files, used for compiling the file as well as to describe the driver's calls to any program using the driver.
- A standard driver library (.LIB) file, to provide the standard functionality all the drivers would require.

This DLL is a set of calls to perform instrument actions — at heart, that's all a VXI*plug&play* driver is — a library of instrument calls.

This driver is accessed by Windows applications programs written in languages such as Visual C++ or Visual BASIC, using programming environments such as VEE or LabView®.

A Windows Help (.HLP) file is included which provides descriptive information and code samples for the functions in the VXI*plug&play* DLL. This help file can be viewed in the standard Windows Help viewer. A viewer for HP-UX is provided in /opt/hyperhelp - see the READ.ME file.

Manufacturer and model codes

If desired, the manufacturer code, model code and name of the VXI instruments can be read from the file :\hpe1432\lib\vximodel.cf (on PC systems) or /opt/e1432/lib/vximodel.cf (on UNIX systems).

The VXI models in this file are as follows:

Manufacturer Code	Model Code	Model Name
0xfff	0x200	Agilent/HP E143xA Non-booted Substrate Board
0xfff	0x201	VT1432A 16 Channel 51.2 kSamples/s Digitizer + DSP
0xfff	0x202	VT1433A 8 Channel 196 kSamples/s Digitizer + DSP
0xfff	0x203	VT1434A 4 Channel 65 kSamples/s Arbitrary Source
0xfff	0x210	VT2216A VXI/SCSI Interface Module

The Soft Front Panel (SFP)

The Soft Front Panel is a stand-alone Windows application, built on top of the VXI*plug&play* driver DLL; it is used for instrument evaluation and debugging and as a demo. It is not a programmable interface to the instrument, nor can it be used to generate code.

The soft front panel also accesses the same Windows Help file as provided with the DLL.

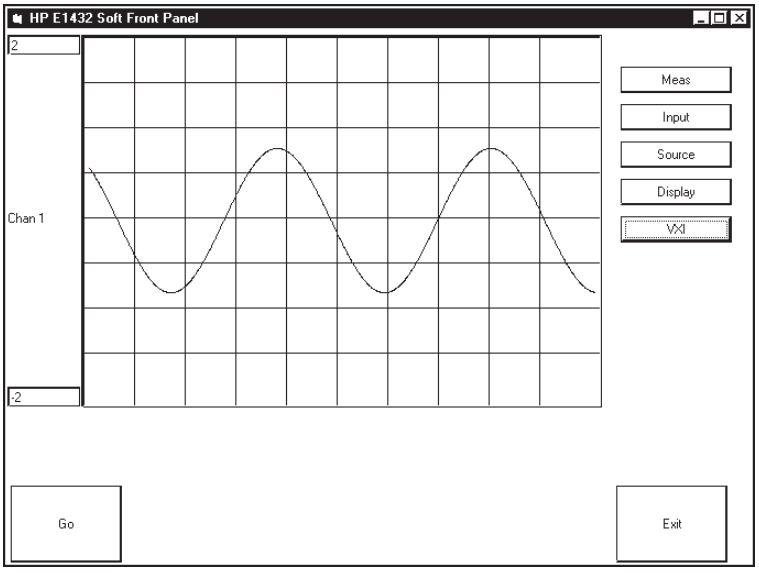


Figure 3-2: An example of a soft front panel (SFP)

Header and Library Files

In the Windows environment, the following files are in the directory \Vxipnp\WinXX\Hpe1432

hpe1432.fp	The “FP” file used by VEE and CVI
hpe1432.hlp	Windows help file
hpe1432.kb	Knowledge base file
hpe1432.bas	header for Visual Basic
hpe1432.exe	Soft front panel program
Bin\hpe1432_32.dll	The VXI*plug&play* driver
Include\hpe1432.h	Header for linking to the VXI*plug&play* driver
Lib\Msc\ hpe1432_32.lib	Lib for linking C programs to VXI*plug&play*

The following files are in the directory \Hpe1432

Read.me	The latest information for the product
lib\sema.bin	Firmware program for the VT1432A
lib\sfp.ico	Icon for help file
lib\sinewave.ico	Icon for Soft Front Panel
source*	Source files for hpe1432_32.dll
examples\vb*	Visual Basic example programs
examples\c*	C example programs
examples\hpvee*	Agilent VEE example programs

In the HP-UX environment, the following files are in the directory /opt/vxipnp/hpux/hpe1432:

hpe1432.fp	The “FP” file used by VEE
.h	Header file
.hlp	Hyperhelp file (see /opt/hyperhelp/README for information on how to view hpe1432.hpl In the HP-UX environment.)
.sl (lower-case “SL”)	The VXI*plug&play* shared library

Programming Considerations

There are some constrains in downloading arb data with the VT1434A, because two channels share a DSP. When both channels of a channel pair (1 & 2, 3 & 4) are active, they share several parameters including signal mode and span (sample rate). When both channels are active, arb data must be downloaded to each channel in chunks the size of the transfer buffers. It is not possible to download all of one channel with multiple transfers, then the next channel. If only channels 1 and 3 are activated, this constraint does not exist. See the example program /opt/e1432/examples/srcparb2.c.

Parameter coupling in the VT1434A

The following parameters are shared by both channels of two-channel source sub-module (SCA). Both channels are set to the same value and the last one set before measure_init will be the one used. To avoid sequence dependency, the setting will occur for a parameter whether the channel referenced is active or not.

- hpe1432_setSourceMode
- hpe1432_setSourceSpan
- hpe1432_setRampRate
- hpe1432_setTriggerChannel
- hpe1432_setSourceBlocksize
- hpe1432_setDutyCycle
- hpe1432_setSourceSeed (internally the sequences for each channel of a DSP are unique)
- hpe1432_setSrcParmMode
- hpe1432_setSrcBufferMode
- hpe1432_setSrcBufferSize
- hpe1432_setSrcBufferInit

The following parameters are NOT shared by the two channels of two-channel source sub module (SCA). They are independent.

- hpe1432_setActive
- hpe1432_setAmpScale
- hpe1432_setRange
- hpe1432_setSourceOutput
- hpe1432_setSineFreq
- hpe1432_setSinePhase
- hpe1432_setCenterFreq (zoomed random)

The following parameters are ignored when sent to the second channel of the two-channel source sub module (SCA).

- hpe1432_setAntiAliasDigital
- hpe1432_setFilterFreq
- hpe1432_setSourceCola

Where to get more information

There is more information available about the VT1434A. This section shows how to access and print it, if desired.

The VT1434A uses the same software as the VT1432A 16 Channel 51.2 kSamples/s Digitizer plus DSP.

The Function Reference for VXI*plug&play*

On a PC: The VT1432A Function Reference is in Microsoft Help text. Select the Help icon in the "VXIPNP" folder. Refer to Microsoft Windows documentation (including Help text) for information on using and printing Help.

On a UNIX system, look at the README file at /opt/hyperhelp. It includes instructions on how to install and use the VXI*plug&play* help.

The Function Reference for the Host Interface Library (C-language version)

The VT1432A distribution includes manual pages for the VT1432A Host Interface library. These manual pages can be examined on-line, using the"ptman" command that is shipped in "/opt/e1432/bin." For example, the manual page for the "e1432_init_measure" function can be read by typing:

ptman e1432_init_measure

The distribution also includes a nicely formatted set of these manual pages,that can be printed on any postscript printer. This manual in postscript form is in file "/opt/e1432/man/man.ps." Typically, this manual can be printed by typing:

lp -opostscript /opt/e1432/man/man.ps

Alternatively, if there is no postscript printer available, a plain text version of the manual is in file "/opt/e1432/man/man.txt." This can be printed on any line printer.

Users of the C-language library will also find useful information about theVT1432A in the VT1432A help text (see above).

4

Module Description

Module Features

The VT1434A 4-Channel 65 kSamples/s Arbitrary Source is a VXI C-sized, arbitrary source module.

An additional arbitrary source channel can be included with the VT1434A 4-Channel 65 kSamples/s Arbitrary Source as Option 1D4. This option can supply an additional channel of arbitrary, random or sine signals under control of measurement software.

The following paragraphs describe features of the VT1434A. See “Specifications” for more detailed information.

Source Output Modes

The Arbitrary Source has several output modes including the following:

- sine wave
- burst sine
- random noise
- burst random noise
- arbitrary

Arbitrary Output

The Arbitrary Source can be programmed to output any signal that is described by data downloaded by the software.

Trigger

The Arbitrary Source can be used to trigger the measurement and to trigger other modules in the measurement system.

COLA

The COLA (Constant Output Level Amplifier) outputs supply a signal similar to the channel 1 and channel 3 source outputs (Ch1 Out and Ch3 Out) except that it is at a constant output level of about 1 volt peak.

External Shutdown

Shorting the center pin of the shutdown connector to its shield causes the source to ramp down and shut off.

Options

The options available for the VT1434A 4-Channel 65 kSamples/s Arbitrary Source include:

1D4	Arbitrary Source (additional channel)
1DM	Two Output Channels (instead of the standard four channels)
ANC	32 MB Total RAM
ANM	4 MB Total RAM
UGV	Local Bus Interface

Block Diagram

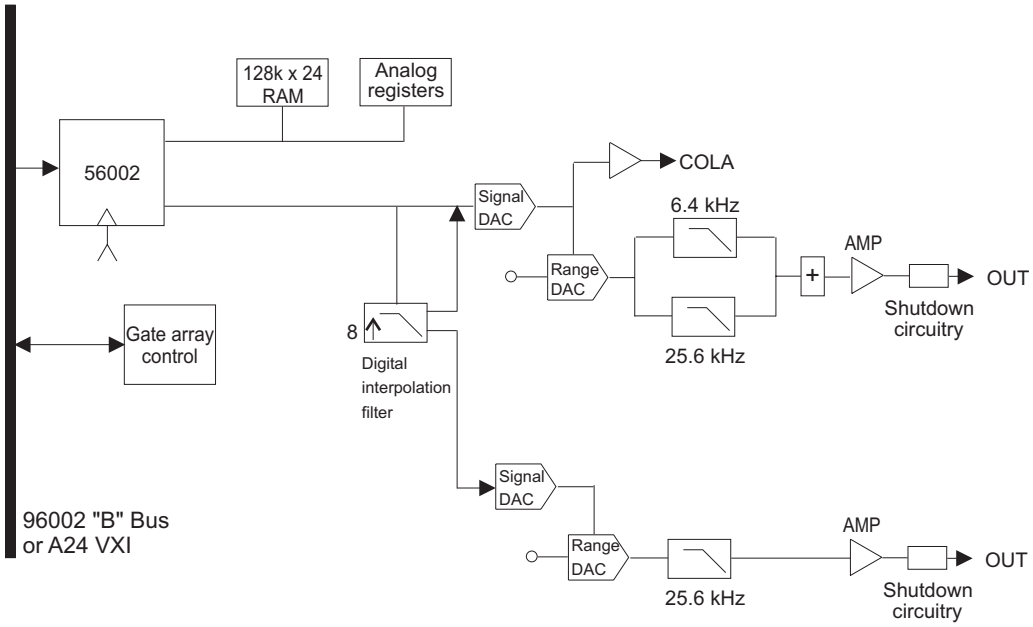


Figure 4-1: Source block diagram

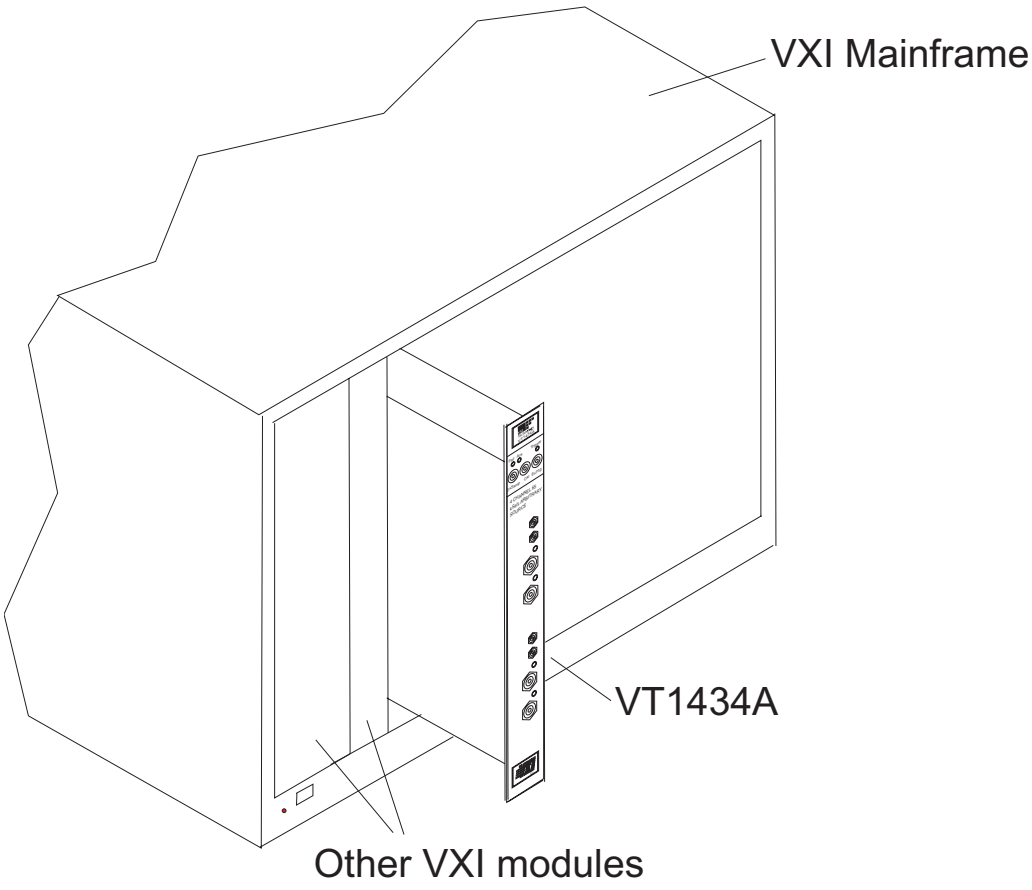


Figure 4-2: The VT1434A in a VXI Mainframe

This a general illustration. See the Chapter 1, Installation for instructions on installing the VT1434A in a mainframe.

VT1434A Front Panel Description

The VT1434A with no options may have two or four outputs. The following illustration shows a front panel with four outputs. The LEDs and connectors are described on the next page.

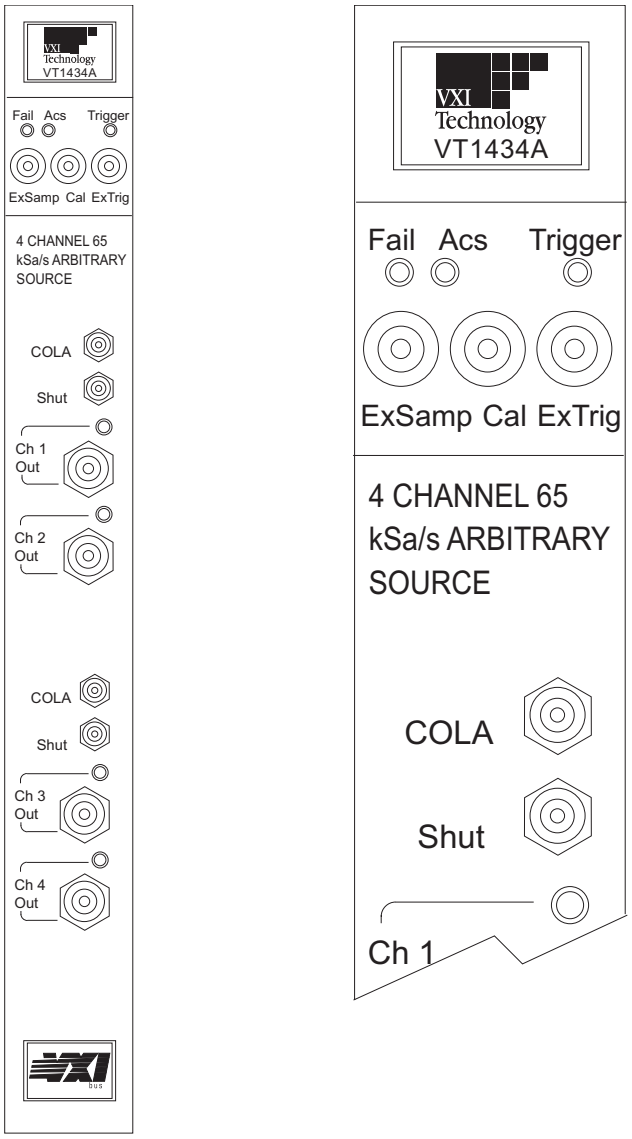


Figure 4-3: VT1434A front panel

LEDs and connectors for the standard VT1434A

Status LEDs

- Fail: This is the standard VXI "Failed" indicator. It lights briefly when powering up and normally goes out after a few seconds. If it stays on it indicates a hardware failure in the module.

- Acs: This is the standard VXI "Access" indicator. When it is on, it indicates that another device on the bus is contacting the module, for example to transfer data or to read registers.

- Trigger: This LED flashes on each time the measurement triggers, so when it is blinking it indicates that the measurement is triggering.

- Output LEDs: These are located next to each output connector. When an output LED is lighted it indicates that the corresponding source channel is on and producing output.

SMB Connectors

- ExSamp: This is an input connector for an external sample clock. The sample clock must be TTL level and have a frequency between 40.96 kHz and 100 kHz. Internally, this frequency can be decimated.

- Cal: This connector is used for calibration. It can be configured to output a calibration signal or to accept an input calibration signal. See the calibration section in this chapter.

- ExTrig: This allows for an external trigger input to the VT1434A. The input signal must be TTL; other characteristics can be defined in software. ExTrig can be enabled or disabled in software.

- COLA: This is the output connector for the COLA (Constant Output Level Amplifier) output. There is a COLA output for each pair of output channels. The COLA output corresponds to the lower-numbered channel of the pair. (That is, channel 1 and channel 3).

- Shut (Shutdown): Shorting the center pin of this connector to its shield causes the source to ramp down and shut off. There is a Shutdown connector for each pair of output channels. When system software is running, any shutdown input will shut down all sources in the system.

Output BNC Connectors

- Out: This is the main output of the Arbitrary Source. There is one output connector for each channel.

  For channels 1 and 3, the Out connector can also be configured to output a calibration signal. This is not quite the same as the calibration signal described in the section on calibration because it comes directly from the internal source without going through the other circuitry of the calibration section.

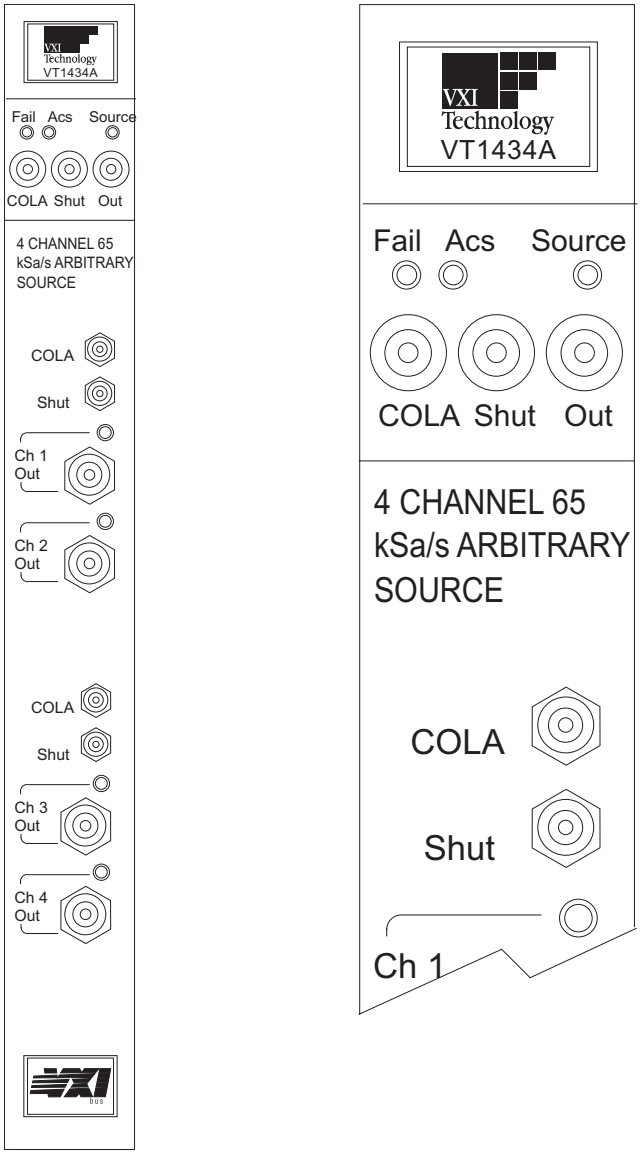


Figure 4-4: Front panel - VT1434A with option 1D4

Additional source channel (option 1D4)

The standard VT1434A has four arbitrary source channels. A fifth channel is added with option 1D4.

The illustration on the previous page shows the front panel for a VT1434A with option 1D4.

LEDs and connectors for the VT1434A with option 1D4

Status LEDs

- Fail: This is the standard VXI "Failed" indicator. It lights briefly when powering up and normally goes out after a few seconds. If it stays on it indicates a hardware failure in the module.

- Acs: This is the standard VXI "Access" indicator. When it is on, it indicates that another device on the bus is contacting the module, for example to transfer data or to read registers.

- Source: If this LED is lighted it indicates that the additional source channel is on and producing output.

SMB Connectors

- COLA: This is the connector for the COLA (Constant Output Level Amplifier) output. There is a COLA output for the additional channel and one for each pair of output channels on the lower part of the front panel. The COLA output is also used as a Summer connector.

- Shut (Shutdown): Shorting the center pin of this connector to its shield causes the source to ramp down and shut off. There is a Shutdown connector for the additional channel and one for each pair of output channels on the lower part of the front panel. When system software is running, any shutdown input will shut down all sources in the system.

- Out: This is the main output for each Arbitrary Source channel. The Out connector for the additional channel is an SMB connector in the upper section of the front panel. For the standard two or four output channels the Out connectors are BNC connectors on the lower part of the front panel.

  For the additional channel, as well as channels 1 and 3, the Out connector can also be configured to output a calibration signal. This is not quite the same as the calibration signal described in the section on calibration because it comes directly from the internal source without going through the other circuitry of the calibration section.

VXI Backplane Connections

Power Supplies and Ground

The VT1434A conforms to the VME and VXI specifications for pin assignment. The current drawn from each supply is given in the specifications chapter.

Data Transfer Bus

The VT1434A conforms to the VME and VXI specifications for pin assignment and protocol. A16, A24, D16 and D32 data transfers are supported.

DTB Arbitration Bus

The VT1434A module is not capable of requesting bus control. Thus it does not use the Arbitration bus. To conform to the VME and VXI specifications, it passes the bus lines through.

Priority Interrupt Bus

The VT1434A generates interrupts by applying a programmable mask to its status bits. The priority of the interrupt is determined by the interrupt priority setting in the control register.

Utility Bus

The VME specification provides a set of lines collectively called the utility bus. Of these lines, the VT1434A only uses the SYSRESET* line.

Pulling the SYSRESET* line low (a hardware reset) has the same effect as setting the reset bit in the Control Register (a software reset), except that pulling the SYSRESET* line low also resets the Control Register itself, while a software reset does not.

The VT1434A VXI Device

Address Space

The VXI system architecture defines two types of address space. A16 space consists of 64 kbytes and A24 consists of 16 Mbytes.

The VT1434A has a 32-bit port through which it has access to the A16 and A24 space. It can also use D32 to send and receive data though the port. Or it can use the port for 16-bit data transfers by using only 16 of the 32 bits available. The VT1434A performs a different type of VME cycle depending on the number of bits transferred per cycle (two cycles for 16-bit transfers and one cycle for 32-bit).

Shared Memory

Shared memory provides a way for the VT1434A to transfer data to a controller. The shared memory in the VT1434A is mapped to the A24 VXI address space. The controller can then access that same address space to receive or write data. A function to can be called to write the data. See the chapter on “The Host Interface Library.”

Memory Map

The following discussion of memory mapping is included as supplementary information. It is not needed to operate the VT1434A because this functionality is hidden when using the VT1434A Host Interface Library software.

The VXI interface maps some of the VT1434A’s internal memory space so that it is visible to the VXI Bus. The VXI bus also has access to the SRAM and DRAM within the module. (SRAM stands for Static RAM; DRAM is Dynamic RAM.)

The VXI interface has two “windows” on the memory space. Each is 128 kbytes, which is 32k 32-bit words. One of the windows is fixed and the other is movable. The movable window allows the VXI bus access to many different parts of the memory space. The fixed window contains:

- The A16 registers
- The B-bus SRAM (on the B-bus within the module)
- The hardware registers

The mapping of the fixed and movable windows is illustrated as follows:

Address		
$3FFFF_{16}$ $2000\ 0_{16}$	Movable DSP Bus Window	Movable
$1FFFF_{16}$ $1000\ 0_{16}$	Send/Receive Data Registers	Fixed
$0FFFF_{16}$ $0004\ F_{16}$	Fixed DSP Bus Window	
$0003\ F_{16}$ $0000\ 0_{16}$	VXIbus A16 Registers	

For more information, see “The A24 Registers” in the chapter titled Register Definitions.

List of A16 Registers

The following lists the A16 registers. For more information see "The A16 Registers" in the chapter titled Register Definitions.

Address	Read	Write
$3E_{16}$	Parameter 7 Register	
$3C_{16}$		
$3A_{16}$	Parameter 6 Register	
38_{16}		
36_{16}	Parameter 5 Register	
34_{16}		
32_{16}	Parameter 4 Register	
30_{16}		
$2E_{16}$	Parameter 3 Register	
$2C_{16}$		
$2A_{16}$	Parameter 2 Register	
28_{16}		
26_{16}	Parameter 1 Register	
24_{16}		
22_{16}	Query Response Register	Command Register
20_{16}		
$1E_{16}$		
$1C_{16}$		
$1A_{16}$	Send Data	
18_{16}		
16_{16}	RAM 1	
14_{16}		
12_{16}	RAM 0	
10_{16}		
$0E_{16}$	IRQ Status Register	IRQ Reset Register
$0C_{16}$	IRQ Config Register	
$0A_{16}$	Page Map Register	
08_{16}	Port Control Register	
06_{16}	Offset Register	
04_{16}	Status Register	Control Register
02_{16}	Device Type	
00_{16}	ID Register	Logical Address Register

Trigger Lines (TTLTRG)

TTLTRG consist of eight TTL lines on the VXI backplane on connector P2. They are available to provide synchronization between devices. VXI devices can use the TTLTRG lines for simple communication with other devices. For example, a device can wait for a line to go high before taking an action or it can assert a line as a signal to another device.

The VT1434A uses two trigger lines. These can be placed on any two of the eight TTLTRG lines available on the VXI backplane. The lines are:

- Sync/Trigger line
- Free-running clock line

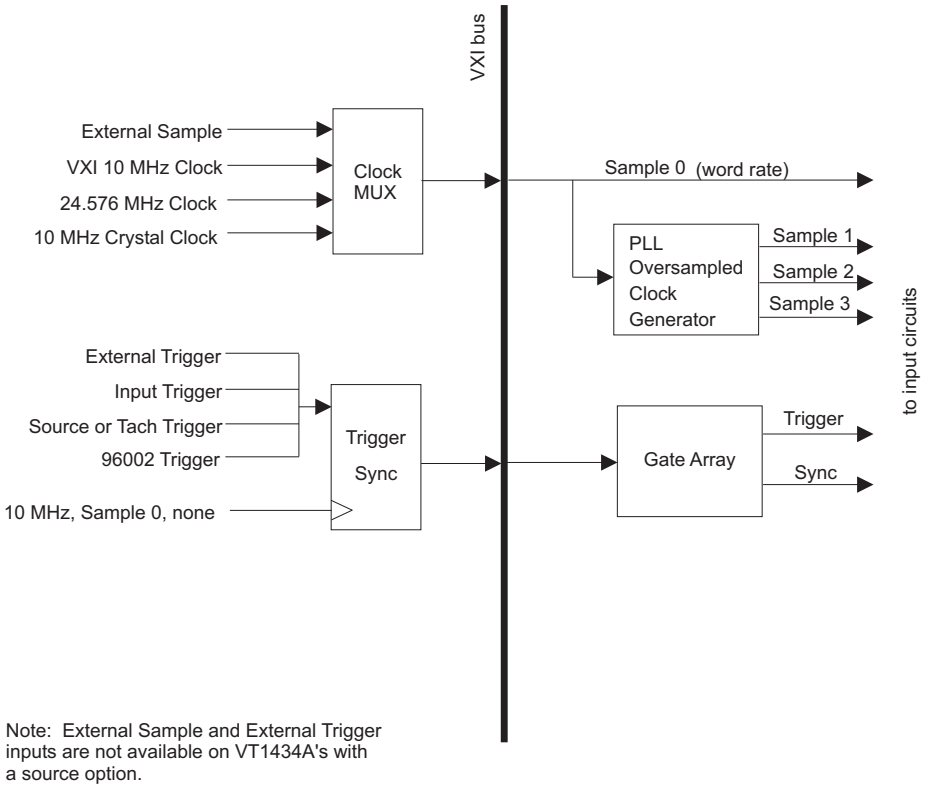


Figure 4-5: Clock/Sync diagram

Providing an External Clock

The VT1434A can be programed to accept an external word rate clock from the Sample 0 line on the VXI bus. The digital filters are still functional, providing a range of effective word rates. All sampling is done simultaneously and is not multiplexed.

To connect an External Sample Clock, use the External Sample SMB connector on front panel of the VT1434A. External Sample at word rate and External Trigger are available on the front panel of VT1434A's which do not have the additional arbitrary source option.

The external clock must be a fixed frequency. Its maximum frequency must not be higher than 65536 Hz. Its minimum frequency must be at least 40960 Hz.

Calibration Description

The Cal connector on the front panel of the standard VT1434A can be configured (in software) as either an input or an output. It can be set to any of four settings:

- DC - The VT1434A outputs a DC calibration signal from the millivolt range up to 15 volts.
- AC - The VT1434A outputs a signal from an Arbitrary Source option (in the same module or a different VT1434A module in the system.)
- Ground - The connector is shunted to ground for a zero-volt reference.
- Open Circuit - In this mode the connector becomes an input which can receive a calibration signal up to ±15 volts.

The VT1434A is calibrated at the factory and the calibration placed in EPROM memory for use at each power-up. In addition an auto-zero function is provided.

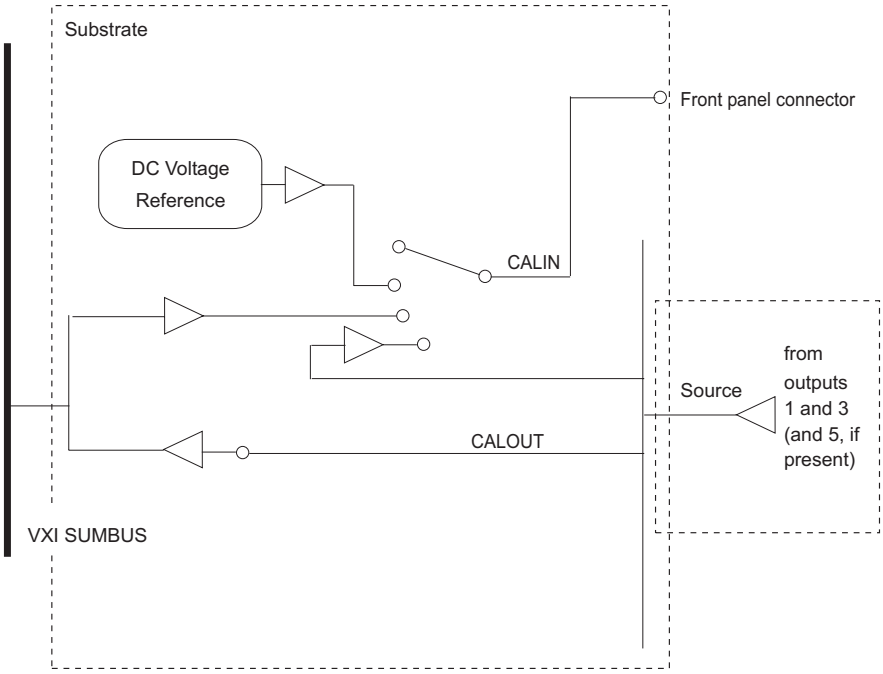


Figure 4-6: Calibration Bock Diagram

5

The Host Interface Library

Introduction

The Host Interface Library for the VT1434A is the same as that used for the VT1432A 16 Channel 51.2 kSamples/s Digitizer plus DSP. It consists of a set of functions that allow the user to program the register-based VT1434A at a higher level than register reads and writes. The library allows groups of VT1434As to be set up and programmed as if they were one entity.

The VT1434A 4-Channel 65 kSamples/s Arbitrary Source does not use any of the library functions that refer to input or tach.

The library includes routines to set up and query parameters, start and stop measurements, read and write data and control interrupts. Routines to aid debugging and perform low-level I/O are also included.

Because the VT1434A uses the same interface library as the VT1432A 16 Channel 51.2 kSamples/s Digitizer plus DSP, the function names begin with "e1432..."

For information on diagnostics see the chapter titled "Troubleshooting the VT1434A."

Almost all functions in the VT1432A library return 0 if they complete successfully and a negative error if there is a problem. The return value of the function should always be checked and appropriate action taken for non-zero values. See the on-line manual pages for more information on error messages.

Header and Library Files

The /opt/e1432/lib directory contains several versions of the VT1432A Host Interface library:

lib1432.a	A normal HP-UX archive library, used by host programs wanting to talk to VT1432A (or VT1434A) hardware.
lib1432.sl	An HP-UX shared library, used by host programs wanting to talk to VT1432A (or VT1434A) hardware. This and the above archive library do exactly the same things. Usually, host programs would use the shared library, because it makes the host program smaller.
llib-l1432.ln	A lint library for the VT1432A host interface library. If lint (a UNIX tool for checking source code for problems) is not used, this file is superfluous.

An application using the VT1432A Host Interface library must link in one of these libraries, typically lib1432.sl. The HP-UX versions of the VT1432A library use SICL to communicate with the VT1432A (or VT1434A) hardware, so an application using the VT1432A library must also link in the SICL library. Normally, this is found in /usr/lib/libsicl.sl.

Any application source code which uses any of the VT1432A Host Interface library functions must include the e1432.h include file, found in /opt/e1432/include. Internally, this file includes machType.h, which is also found in /opt/e1432/include. If the application refers to specific VT1432A or VT1434A error numbers, it must also include err1432.h.

VT1434A Interrupt Behavior

Interrupt Setup

The VT1434A VXI module can be programmed to interrupt a host computer using the VME interrupt lines. VME provides seven such lines and the VT1434A module can be told to use any one of them (see e1432_set_interrupt_priority).

The VT1434A can interrupt the host computer in response to different events. The user can specify a mask of events on which to interrupt. This mask is created by OR'ing together the various conditions that the user wants. The following table, copied from the e1432_set_interrupt_mask manual page, shows the conditions that can cause an interrupt:

Interrupt Mask Bit Definitions

Define (in e1432.h)	Description
E1432_IRQ_MEAS_STATE_CHANGE	Measurement state machine changed state
E1432_IRQ_SRC_STATUS	Source status change

VT1434A Interrupt Handling

To make the VT1434A module do the interrupt, both a mask and a VME Interrupt line must be specified, by calling e1432_set_interrupt_mask and e1432_set_interrupt_priority respectively. Once the mask and line have been set and an interrupt occurs, the cause of the interrupt can be obtained by reading the E1432_IRQ_STATUS_REG register (using e1432_read_register). The bit positions of the interrupt mask and status registers match so the defines can be used to set and check IRQ bits.

Once it has done this interrupt, the module will not do any more VME interrupts until re-enabled with e1432_reenable_interrupt. Normally, the last thing a host computer's interrupt handler should do is call e1432_reenable_interrupt.

Events that would have caused an interrupt, but which are blocked because e1432_reenable_interrupt has not yet been called, will be saved. After e1432_reenable_interrupt is called, these saved events will cause an interrupt, so that there is no way for the host to "miss" an interrupt. However, the module will only do one VME interrupt for all of the saved events, so that the host computer will not get flooded with too many interrupts.

Host Interrupt Setup

The VT1432A Host Interface library normally uses the SICL I/O library to communicate with the VT1434A hardware. To receive VME interrupts, a variety of SICL setup calls must be made. The “examples” directory of the VT1434A distribution contains an example of setting up SICL to receive interrupts from a VT1434A module.

This is a summary of how to set up SICL to receive a VT1434A interrupt:

- Query SICL for which VME interrupt lines are available, using ivxibusstatus and ivxirminfo.
- Tell the VT1434A module to use the VME interrupt line found in step one, using e1432_set_interrupt_priority.
- Set up an interrupt handler routine, using ionintr and isetintr. The interrupt handler routine will get called when the interrupt occurs.
- Set up interrupt mask in the VT1434A module, using e1432_set_interrupt_mask.

Host Interrupt Handling

When the VT1434A asserts the VME interrupt line, SICL will cause the specified interrupt handler to get called. Typically the interrupt handler routine will read data from the module and then re-enable VT1434A interrupts with e1432_reenable_interrupt. The call to e1432_reenable_interrupt must be done unless the host is not interested in any more interrupts.

Inside the interrupt handler, almost any VT1432A Host Interface library function can be called. This works because the Host Interface library disables interrupts around critical sections of code, ensuring that communication with the VT1434A module stays consistent. Things that are not valid in the handler are:

- Calling e1432_delete_channel_group to delete a group that is simultaneously being used by non-interrupt-handler code.
- Calling e1432_assign_channel_numbers to reset the list of channels that are available to the VT1432A library.

As is always the case with interrupt handlers, it is easy to introduce bugs into a program and generally difficult to track then down. Be careful when writing this function.

Parameter Information

Description of VT1434A Parameters

Some parameters, such as range or coupling, apply to specific channels. When a channel ID is given to a function that sets a channel-specific parameter, only that channel is set to the new value.

Some parameters, such as clock frequency or data transfer mode, apply globally to a module. When a channel ID is used to change a parameter that applies to a whole module, the channel ID is used to determine which module. The parameter is then changed for that module.

Starting and stopping a measurement is somewhat like setting a global parameter. Starting a measurement starts each active channel in each module that has a channel in the group.

After firmware is installed and after a call to e1432_preset, all of the parameters (both channel-specific and global) in a VT1434A module are set to their default values. For channel-specific parameters, the default value may depend on the type of channel. Some channel-specific parameters apply only to a specific type of channel. For example, tach holdoff applies only to tach channels. Setting such a parameter for a channel that doesn't make sense will result in an error.

At the start of a measurement, the VT1434A firmware sets up all hardware parameters and ensures that the input hardware is settled before starting to take data. The firmware also ensures that any digital filters have time to settle. This ensures that all data read from the module will be valid.

However, after a measurement starts, VT1434A parameters can still be changed. The effect of this change varies, depending on the parameter. For some parameters, changing the value immediately aborts the measurement. For other parameters, the measurement is not aborted, but the changed parameter value is saved and not used until a new measurement is started. For still other parameters, the parameter change takes place immediately and the data coming from the module may contain glitches or other effects from changing the parameter.

Parameter Lists

This section shows which parameters are global parameters, which are channel-specific and what types of channels the channel-specific parameters apply to. Default values are shown for all of these parameters. In addition, each parameter is categorized as “abort”, “wait”, “immediate” or “glitch” depending on the behavior when this parameter is changed during a running measurement. Those with “abort” cause the measurement to abort. Those with “wait” don’t take effect until the start of the next measurement. Those with “immediate” take effect immediately. Those with “glitch” take effect immediately and may cause glitches in the data that is read back or on the source output if the parameter is applied to a source channel.

Global Parameters

Parameter	Default Value	Changes
arm_mode	Auto Arm	Immediate
auto_trigger	Auto Trigger	Abort
blocksize	1024	Abort
cal_dac	0	Immediate
cal_voltage	0 volts	Immediate
calin	Grounded	Immediate
clock_freq	51.2 kHz	Abort
clock_master	Off	Abort
clock_source	Internal	Abort
internal_debug	0x100	Immediate
interrupt_mask	0	Immediate
interrupt_priority	None	Immediate
multi_sync	Off	Abort
pre_arm_mode	Auto Arm	Immediate
span	20000 Hz	Wait
sumbus	Off	Immediate
trigger_ext	Off	Immediate
triggers_per_arm	1	Immediate
ttltrg_clock	TTLTRG1	Abort
ttltrg_gclock	TTLTRG1	Abort
ttltrg_satrg	TTLTRG0	Abort
ttltrg_trigger	TTLTRG0	Abort

Source Parameters (and option 1D4 parameters)

Parameter	Default Value	Changes	VT1434A Coupled*
active	Off	Abort	No
amp_scale	1.0	Immediate**	No
anti_alias_digital	On	Wait	1 Channel
duty_cycle	0.5	Wait	Yes
filter_freq	25.6 kHz	Wait	1 Channel
ramp_rate	1 second	Wait	Yes
range	0.041567 Volt	Glitch	No
sine_freq	1 kHz	Immediate	No
sine_phase	0 Degrees	Glitch	No
source_blocksize	0 (Use input blocksize)	Wait	Yes
source_centerfreq	250 Hz	Wait	No
source_cola	Off	Wait	1 Channel
source_mode	Sine	Abort	Yes
source_output	Normal	Abort	No
source_seed	3	Wait	Yes***
source_span	0 (Use input span)	Wait	Yes
source_sum	Off	Wait	1 Channel
srcbuffer_init	Empty	Wait	Yes
srcbuffer_mode	Periodic	Wait	Yes
srcbuffer_size	1024	Wait	Yes
srcparm_mode	Immediate	Immediate	Yes
trigger_channel	Off	Wait	Yes

*VT1434A channels are in pairs. For the parameters for which “VT1434A Coupled” is “yes” the settings for both channels in a pair must be the same.

**If the sample rate is greater than 51200 samples per second and both channels of the SCA are active this change is “Wait,” otherwise it is “Immediate.”

***The single shared value of source seed generates unique sequences on the two VT1434A channels.

Channel and Group IDs

Most functions in the VT1432A Host Interface Library take an ID parameter which specifies what channel or group of channels the function should apply to. The ID can either be a channel ID or a group ID. If a group ID is used, then the function is applied to each channel contained in the group.

Channel IDs

Channel IDs are logical IDs which are created by a call to e1432_assign_channel_numbers. The e1432_assign_channel_numbers function must be called exactly once, following the call to e1432_init_io_driver, in order to declare to the library the logical addresses of the VT1434A modules that will be used.

This function checks the existence of a VT1434A module at each of the logical addresses given in a list of logical addresses and allocates logical channel identifiers for each channel in all of the VT1434As. Input channels, source channels and tach/trigger channels are kept logically separated. (Only source channels apply to the VT1434A.) Channel numbers for each type of channel are numbered starting from one, so there will be input channels 1 through M, source channels 1 through N and tach/trigger channels 1 through P, where M is the number of input channels, N is the number of source channels and P is the number of tach/trigger channels.

As an example, suppose two logical addresses 100 and 101 are passed to the function. Suppose that the logical address 100 refers to a VT1432A which has two 4-channel input SCAs and a 1-channel source board, while logical address 101 refers to a VT1434A which has four source SCAs and an additional 1-channel source board. In this case, input channel IDs 1 through 8 are assigned to the eight input channels at logical address 100, while source channel ID 1 is assigned to the one source channel at logical address 100. Source channel IDs number 2 through 6 are assigned to the five source channels at logical address 101.

To use the ID of an input channel, the input channel number is given as an argument to the E1432_INPUT_CHAN() macro. (For backwards compatibility with the Agilent/HP E1431, the macro currently does nothing.) To use the ID of a source channel, the source channel number is given as an argument to the E1432_SOURCE_CHAN() macro. To use the ID of a tach/trigger channel, the tach/trigger channel number is given as an argument to the E1432_TACH_CHAN() macro. A channel ID is always positive.

For example, to set the range of the third input channel to 10 volts, the source code would look something like:

```
status = e1432_set_range(hwid, E1432_INPUT_CHAN(3), 10.0);
```

Group IDs

Group IDs are logical IDs which are created by a call to e1432_create_channel_group. This function can be called multiple times to create multiple groups and each group can contain any combination of channels, including mixtures of different types of channels. The channel groups can overlap as well.

This function creates and initializes a channel group. A channel group allows commands to be issued to several VT1434A channels at once, simplifying system setup. The state of an individual VT1434A channel that is in more than one channel group, is determined by the most recent operation performed on any group to which this channel belongs.

If successful, this function returns the ID of the group that was created, which is then used to reference the channel group in most other functions in this library. A group ID is always negative.

As a side effect, this function makes all input channels in the channel group active and all source and tach channels in the channel group inactive. Unlike the Agilent/HP E1431 library, this function does not inactivate other channels within the modules that the channels are in. Also unlike the Agilent/HP E1431 library, this function does not preset the channels in the new group.

As an example, to create a group consisting of the first three input channels and the eighth and ninth input channels, the code would like something like this:

```
SHORTSIZ16 chan_list[5];
SHORTSIZ16 input_group;
chan_list[0] = E1432_INPUT_CHAN(1);
chan_list[1] = E1432_INPUT_CHAN(2);
chan_list[2] = E1432_INPUT_CHAN(3);
chan_list[3] = E1432_INPUT_CHAN(8);
chan_list[4] = E1432_INPUT_CHAN(9);
input_group = e1432_create_channel_group(hw, 5, chan_list);
```

To create a group consisting of the first two source channels, the code would look something like this:

```
SHORTSIZ16 chan_list[2];
SHORTSIZ16 source_group;
chan_list[0] = E1432_SOURCE_CHAN(1);
chan_list[1] = E1432_SOURCE_CHAN(2);
source_group = e1432_create_channel_group(hw, 2, chan_list);
```

Channel Parameters vs. Module Parameters

Some parameters, such as range or coupling, apply to specific channels. When a channel ID is given to a function that sets a channel-specific parameter, only that channel is set to the new value. When a group ID is given to a function that sets a channel-specific parameter, all channels in the group are set to the new value.

Some parameters, such as clock frequency or data transfer mode, apply to a module. When a channel ID is given to a function that applies to a whole module, the channel ID is used to determine which module. The parameter is then changed for that module. When a group ID is given to a function that applies to a whole module, the function is applied to each module that contains a channel in the group.

Starting and stopping a measurement is somewhat like setting a module-specific parameter. Starting a measurement starts each active channel in each module that has a channel in the group.

For More Information

Refer to the (on-line) VT1432A Function Reference for a list of all functions and the parameters needed for each function. (See “Where to get more information” in the chapter titled “Using the VT1434A”).

Examples

Example and Demo Programs

The VT1432A Host Interface library, which is used to control the VT1434A comes with several example and demo programs, which help demonstrate how to use the library. These programs are found in the "/opt/e1432/examples" directory and the "/opt/e1432/demo" directory. The example programs are very small, so that they will be easily understood and easy to copy into a real application.

Example and demo programs that use the VT1434A source include:

- /opt/e1432/examples/srcparb2.c
- /opt/e1432/demo/semascope2.c
- /opt/e1432/demo/semascope3.c

6

Troubleshooting the VT1434A

Diagnostics

The following describes a limited diagnostic program for the VT1432A, VT1433B and VT1434A. It is to be run from an HP-UX host. The program is called "hostdiag." It can be found with the VT1432A Host Interface Software Library at location /usr/e1432/bin.

location: /usr/e1432/bin

Usage: hostdiag [-hPsuvV] [-f file] [-L laddr] [-S slot] [-O list]

-h
Does a quick, partial test by bypassing the tests which involve downloading code to the module.

-f file
Uses "file" as the source of code to download to the module instead of the default sema.bin.

-L logical_addr
Specifies the logical address of the module to be tested. The default value is 8.

-O option_list
Tests the module against a list model/options. For example -O "E1432,1DE,AYF" tests the module as an eight channel VT1432A with the tachometer option. Without this option, hostdiag only tests what it finds present. Hardware which has failed in such a way that it appears to be absent will not be detected without this option.

-P
Prints only a pass/fail message - no diagnostic printouts.

-s
Additionally runs the "standard input/output" tests. Sources finish testing with 1 V_{PK}, 1 kHz sine on each output for manual verification of output functionality. Input testing (both VT1432A and VT1433B inputs and the Tachometer input) assumes 1 V_{PK}, 1 kHz sine input on each channel. This allows testing of additional portions of the signal path which inaccessible from the internal tests.

-S vxi_slot
Test the module in the vxi slot, vxi_slot. Default is to test the module at logical address 8.

-u
Display usage message.

-v
Specifies the verbose printing. Normally, hostdiag does not print anything unless an error is found. With this option, hostdiag prints status messages as it operates. This option also enables additional diagnostic information which is not generally useful.

-V
Print version info.

Hostdiag returns 0 upon success or returns non-zero if an error is detected.

Coverage:

- Main board
- DRAM SIMMs
- Input SCAs (Signal Conditioning Assemblies)
- Source SCAs (VT1434A)
- Optional source
- Optional tachometer (VT1432A and VT1433B)

Notes:

- Tests are somewhat limited but will catch many hardware errors
- No errors printed means that all tests passed

7

Replacing Assemblies

Replaceable Parts

For information on upgrading the module or replacing parts, contact a VXI Technology sales and service office. See the inside back cover of this guide for a list of office locations and address.

Replacement parts are listed in the following tables:

- Assemblies: without option 1D4
- Assemblies: with option 1D4
- Cables: without option 1D4
- Cables: with option 1D4
- Front Panel

Ordering Information

To order a part listed in one of the tables, quote the VXI Technology part number (VTI Part Number), indicate the quantity required and address the order to the nearest VXI Technology sales and service office (see the inside back cover of this guide). The first time a part is listed in the table, the quantity column (Qty) lists the total quantity of the part used in the module. For the corresponding name and address of the manufacturer's CAGE codes shown in the tables, see "CAGE Code Numbers."

Caution

The module is static sensitive. Use the appropriate precautions when removing, handling and installing to avoid unnecessary damage.

Direct Mail Order System

Within the U.S.A., VXI Technology can supply parts through a direct mail order system. Advantages of the Direct Mail Order System are:

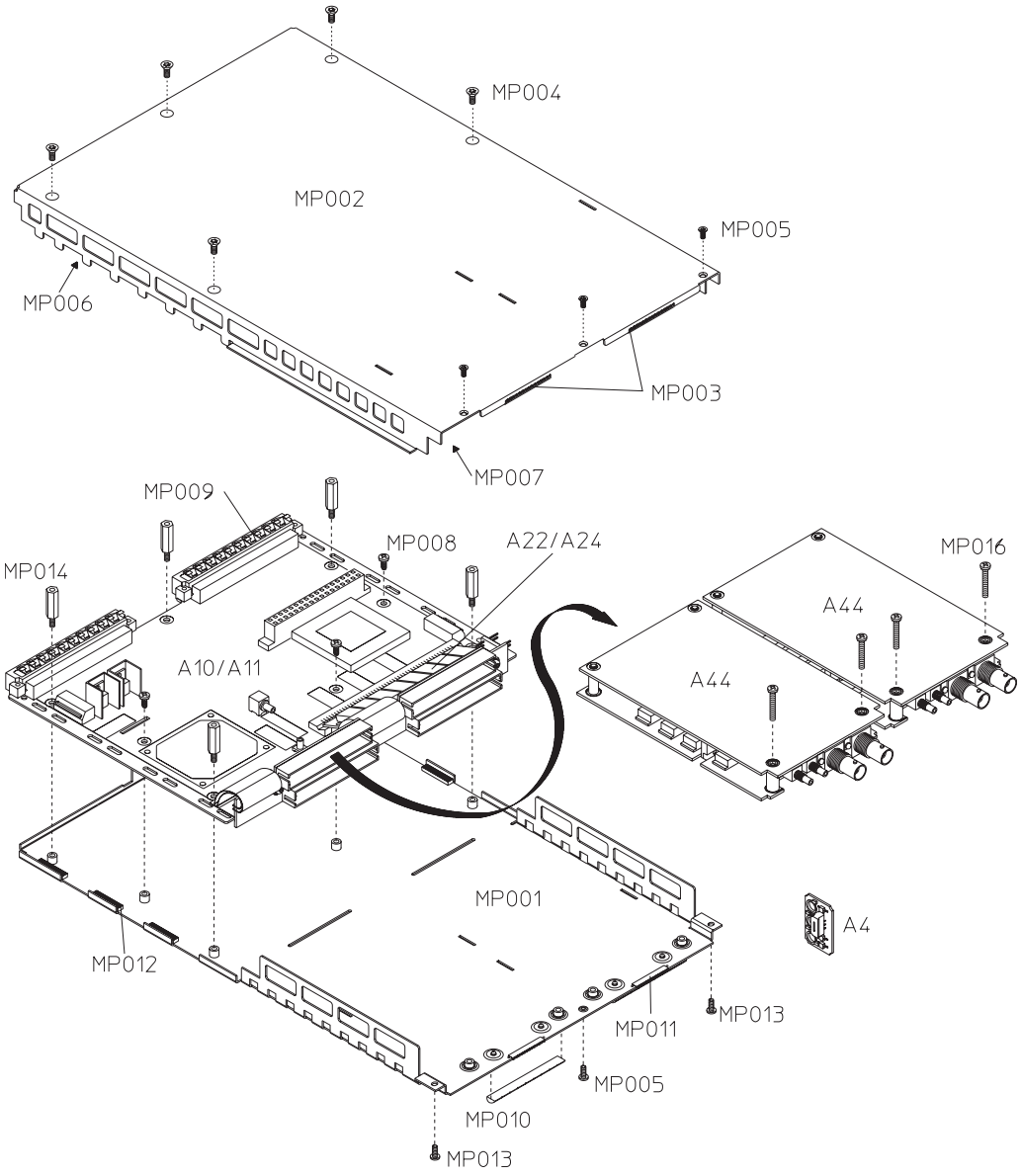
- Direct ordering and shipment from VXI Technology.
- No maximum or minimum on any mail order. There is a minimum order for parts ordered through a VXI Technology sales and service office when the orders require billing and invoicing.
- Transportation charges are prepaid. A small handling charge is added to each order.
- No invoicing. A check or money order must accompany each order.
- Mail order forms and specific ordering information are available through a VXI Technology sales and service office. See the inside back cover of this guide for a list of VXI Technology sales and service office locations and addresses.

CAGE Code Numbers

The following table provides the name and address for the manufacturers' CAGE code numbers (Mfr Code) listed in the replaceable parts tables.

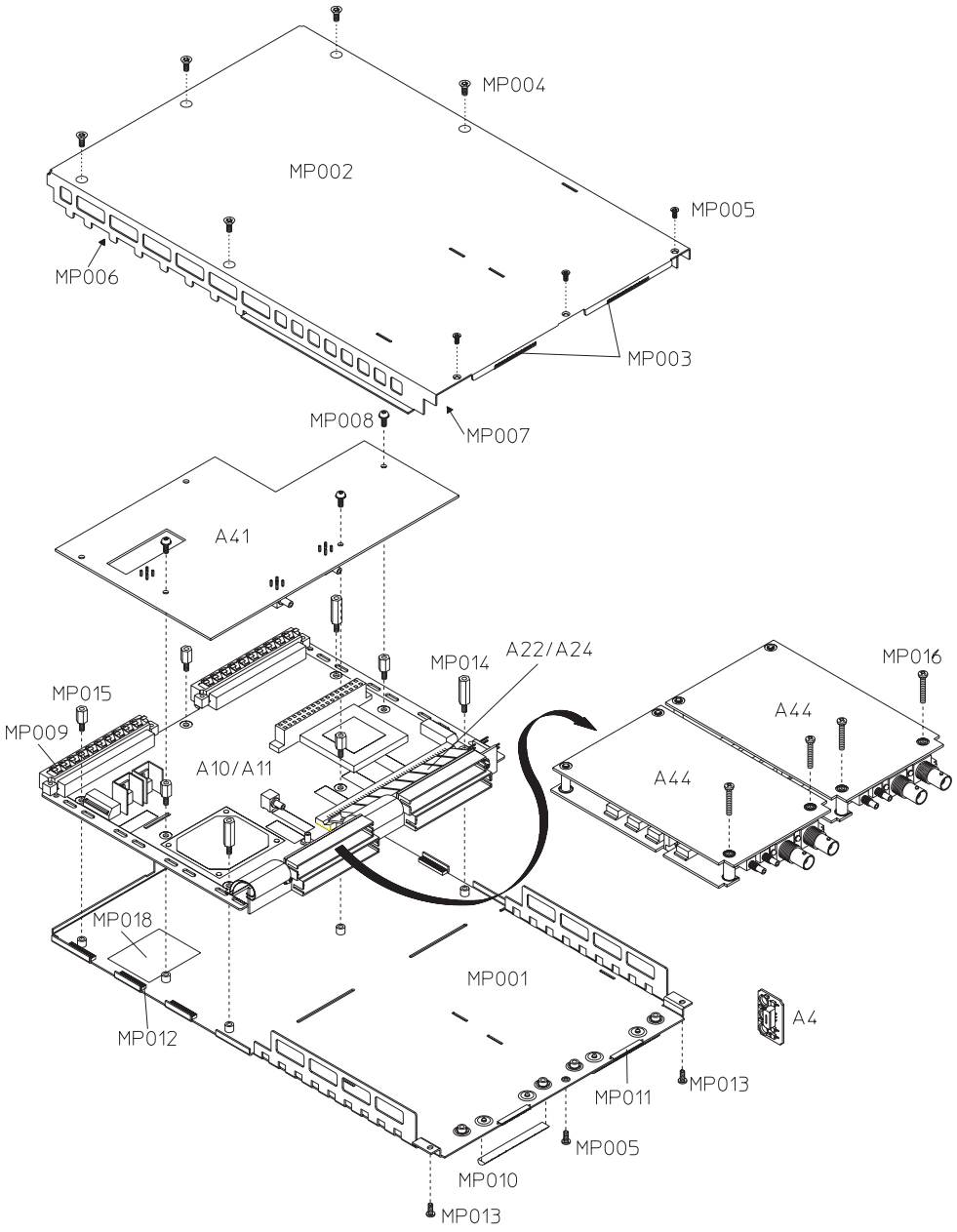
Mfr Code	Mfr Name	Address
03LB1	VXI Technology, Inc.	Irvine, CA U.S.A.
22526	FCI USA Inc.	Etters, PA U.S.A.
30817	Laird Technologies	Delaware Water Gap, PA U.S.A.
83486	Elco Industries Inc.	Rockford, IL U.S.A.
96341	M/A-COM Inc.	Lowell, MA U.S.A.

Assemblies: without option 1D4



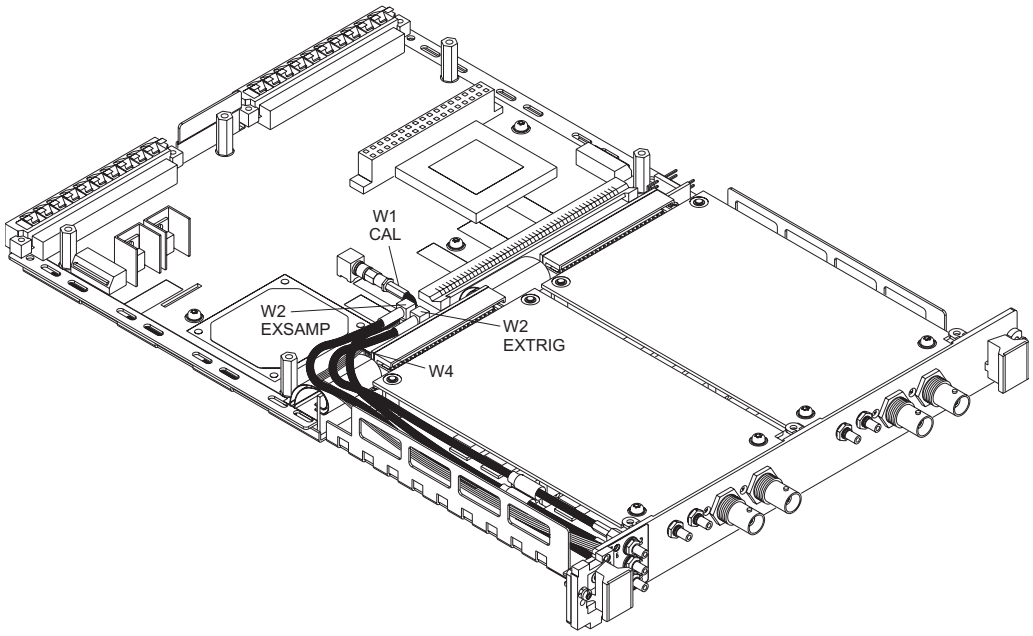
Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
A4	E1432-66504	1	PC ASSY-LED	03LB1	E1434-66504
A10	E1433-66510	1	PC ASSY-MAIN UGV	03LB1	E1433-66510
A11	E1433-66511	1	PC ASSY-MAIN	03LB1	E1434-66511
A22	1818-5622	1	ICM DRAM, SIMM, 8M	03LB1	1818-5622
A24	1818-5624	1	ICM DRAM, SIMM, 1M	03LB1	1818-5624
A44	E1434-66544	2	PCA MAIN	03LB1	E1434-66544
MP001	E1432-00601	1	SHTF CVR-BTTM ALSK	03LB1	E1432-00601
MP002	E1432-00603	1	SHTF CVR-TOP	03LB1	E1432-00603
MP003	8160-0862	0	GSKT RFI STRIP FNGRS	30817	0097-553-17-020
MP004	0515-2033	5	SCR-MCH M3.0 10MMLG	03LB1	0515-2033
MP005	0515-2028	4	SCR-MCH M2.5 6MMLG	03LB1	0515-2028
MP006	E1432-44101	1	GSKT THERMAL CONDUCTOR	03LB1	E14320-44101
MP007	E1485-40601	1	GSKT-RFT, TOP CVR ADH SHT	03LB1	E1485-40601
MP008	0515-0372	3	SCR-MCH M3.0 8MMLG	03LB1	0515-0372
MP009	E1450-01202	4	STMP SHLD-RFI GRND	03LB1	E1450-01202
MP010	8160-0686	1	STMP FNGRS-RFI STRP BECU	30817	786-185
MP011	8160-0683	0	STMP STRP-SPNG FLTR GRD	30817	0097-551-17-X
MP012	8160-0869	6	GSKT RFI, 2MM X 4MM	03LB1	8160-0869
MP013	0515-0368	2	SCR-MCH M2.5 X 0.45	03LB1	0515-0368
MP014	0380-4042	5	STDF-HXMF M3.0 16.7MMLG	03LB1	0515-4042
MP016	0515-2383	4	SCR-MCH M2.5 X 5	03LB1	0515-2383

Assemblies: with option 1D4



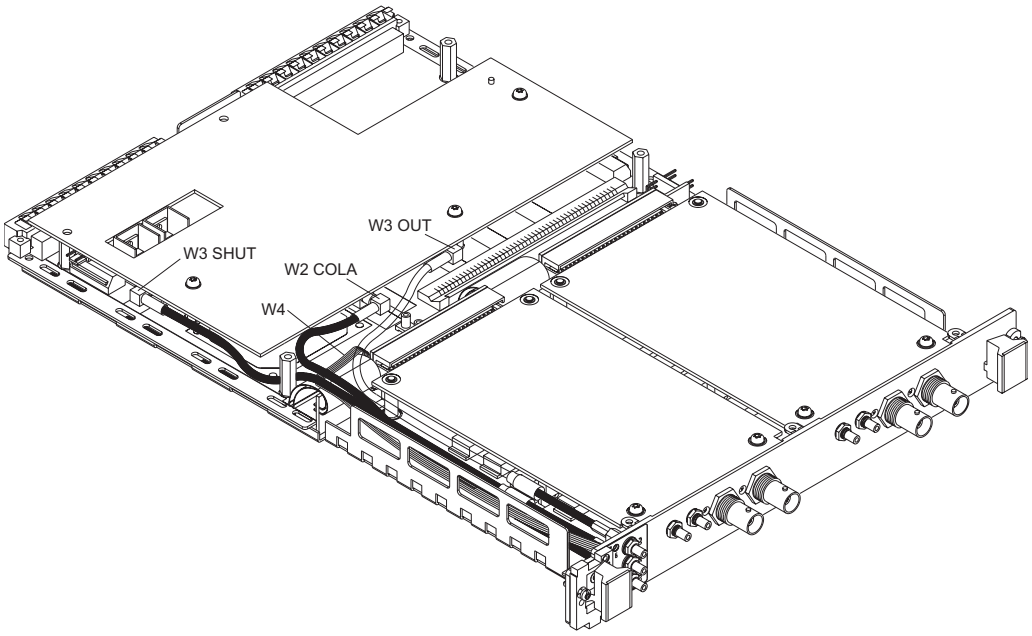
Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
A4	E1434-66504	1	PC ASSY-LED	03LB1	E1434-66504
A10	E1433-66510	1	PC ASSY_MAIN UGV	03LB1	E1433-66510
A11	E1434-66511	1	PC ASSY-VXI INPUT NO LCL BUS	03LB1	E1434-66511
A22	1818-5622	1	ICM DRAM, SIMM, 8M	03LB1	1818-5622
A24	1818-5624	1	ICM DRAM, SIMM, 1M	03LB1	1818-5624
A41	E1432-66541	1	PC ASSY-OPT 1D4	03LB1	E1432-66541
A44	E1434-66544	2	PCA MAIN	03LB1	E1434-66544
MP001	E1432-00601	1	SHTF CVR-BTTM ALSK	03LB1	E1432-00601
MP002	E1432-00603	1	SHTF CVR-TOP	03LB1	E1432-00603
MP003	8160-0862	0	GSKT RFI STRIP FNGRS	30817	0097-553-17-020
MP004	0515-2033	5	SCR-MCH M3.0 10MMLG	03LB1	0515-2033
MP005	0515-2028	4	SCR-MCH M2.5 6MMLG	03LB1	0515-2028
MP006	E1432-44101	1	GSKT THERMAL CONDUCTOR	03LB1	E14320-44101
MP007	E1485-40601	1	GSKT-RFT, TOP CVR ADH SHT	03LB1	E1485-40601
MP008	0515-0372	3	SCR-MCH M3.0 8MMLG	03LB1	0515-0372
MP009	E1450-01202	4	STMP SHLD-RFI GRND	03LB1	E1450-01202
MP010	8160-0686	1	STMP FNGRS-RFI STRP BECU	30817	786-185
MP011	8160-0683	0	STMP STRP-SPNG FLTR GRD	30817	0097-551-17-X
MP012	8160-0869	6	GSKT RFI, 2MM X 4MM	03LB1	8160-0869
MP013	0515-0368	2	SCR-MCH M2.5 X 0.45	03LB1	0515-0368
MP014	0380-4042	3	STDF-HXMF M3.0 16.7MMLG	03LB1	0515-4042
MP015	0380-4041	5	STDF-HXME M3.0	03LB1	0515-4041
MP016	0515-2383	4	SCR-MCH M2.5 X 5	03LB1	0515-2383

Cables: without option 1D4



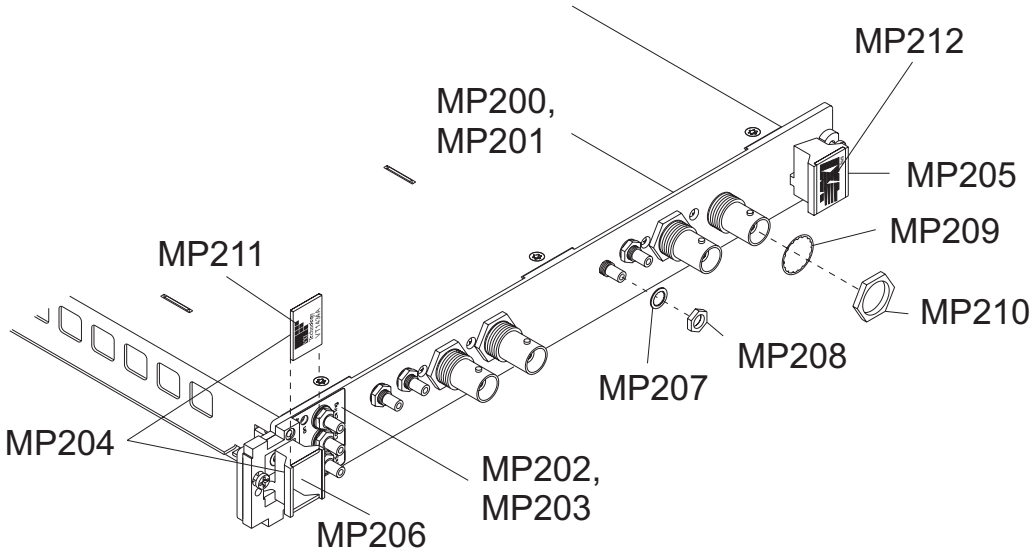
Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
W1	8120-6767	1	CBL-ASM CXL, 290MM	03LB1	8120-6767
W2	8120-6765	2	CBL-ASM CXL, 255MM	03LB1	8120-6765
W4	8120-6762	1	CBL-FLEX, 5-COND, 225MML	03LB1	8120-6762

Cables: with option 1D4



Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
W2	8120-6765	1	CBL-ASM CXL, 255MM	03LB1	8120-6765
W3	8120-6766	2	CBL-ASM CXL,	03LB1	8120-6766
W4	8120-6762	1	CBL-FLEX, 5-COND, 225MML	03LB1	8120-6762

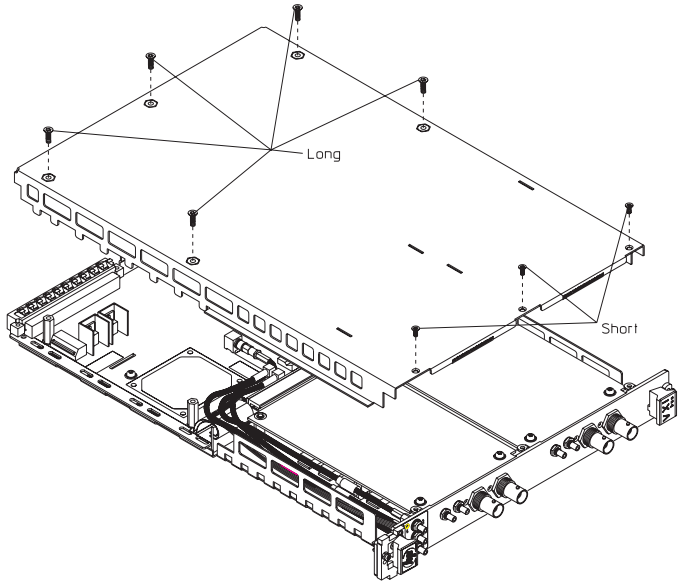
Front Panel



Ref Des	VTI Part Number	Qty	Description	Mfr Code	Mfr Part Number
MP200	E1434-00208	1	PNL-FRT, STANDARD	03LB1	E1432-00204
MP201	E1432-00207	1	PNL-FRT, OPT 1DM	03LB1	E1432-00202
MP202	E1432-44301	1	LBL-FRT PNL SMB'S, STD	03LB1	E1432-44301
MP203	E1432-44302	1	LBL-FRT PNL SMB'S, OPT 1D4	03LB1	E1432-44302
MP204	E1400-84106	1	MOLD KIT-TOP EXTR HNDL	03LB1	E1400-84106
MP205	E1400-84105	1	MOLD KIT-BTTM EXTR HNDL	03LB1	E1400-84105
MP206	0515-1375	2	SCR-MCH M2.5 6MMLG	03LB1	0515-1375
MP207	2190-0124	4	WSHR-LK #10 NTT	96341	500222
MP208	2950-0078	4	NUT-HXP 10-32	22526	HN100-11
MP209	2190-0068	4	WSHR-LK 0.50 NTT	03LB1	2190-0068
MP210	2950-0154	4	NUT-HXP 0.5-28	03LB1	2950-0154
MP211	43-0016-003	1	LABEL, VXI EXT, VXI TECH, NEW LOGO	03LB1	43-0016-003
MP212	43-0016-003	1	LABEL, VXI EXT, VXIBUS	03LB1	43-0016-002

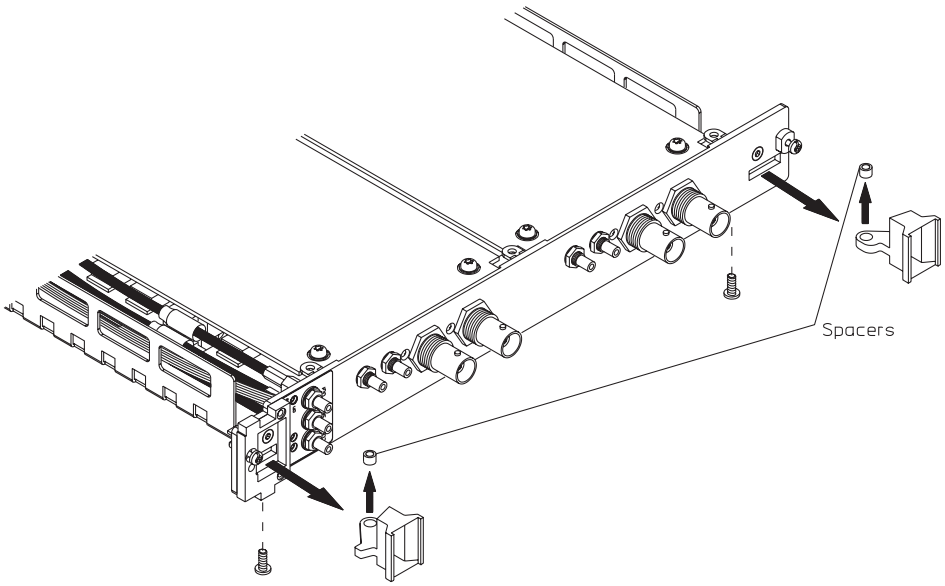
To remove the top cover

1 Remove the five long screws using a T-10 Torx driver and remove the three short screws using a T-8 Torx driver. Lift cover off.

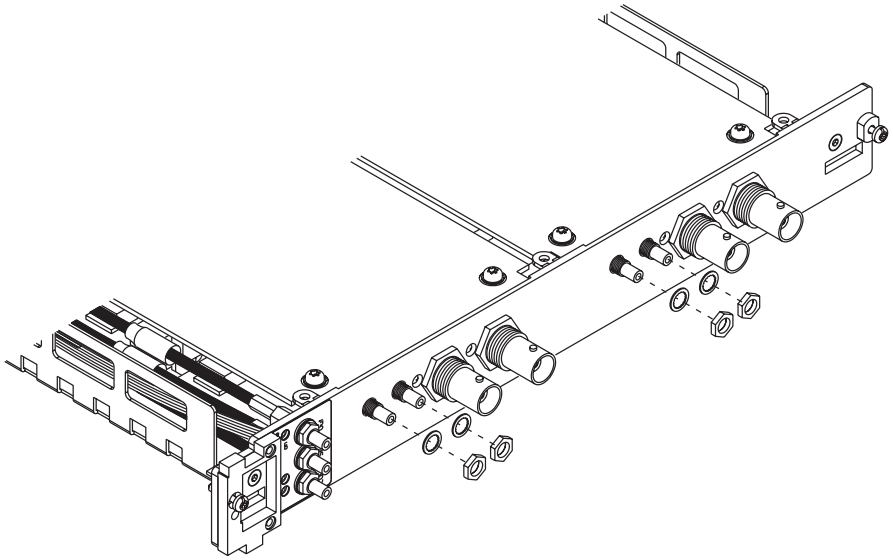


To remove the front panel

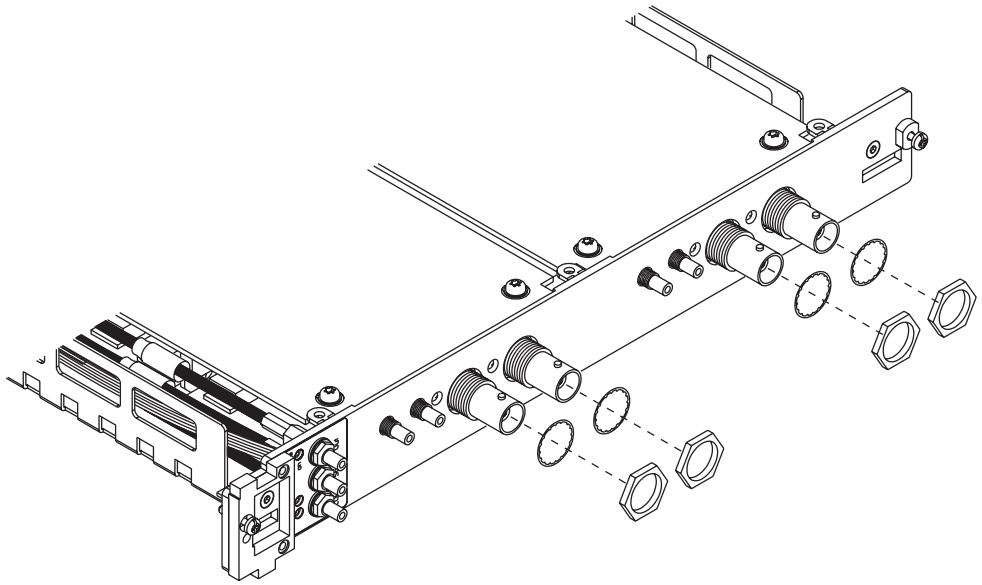
1 Remove top cover, see “To remove the top cover.” Gently disconnect cables from the printed circuit assemblies. Using a T-8 Torx driver, remove the two screws that attach the handles to the assembly. Pull out the handles making sure not to lose the two spacers.



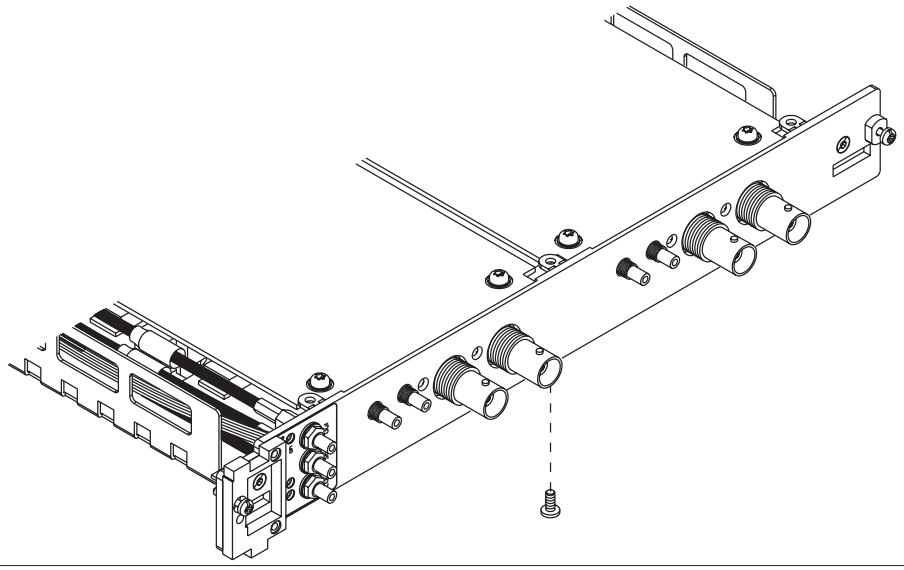
2 Using a 1/4" nut driver, remove the four nuts and washers form the gold connectors as shown.



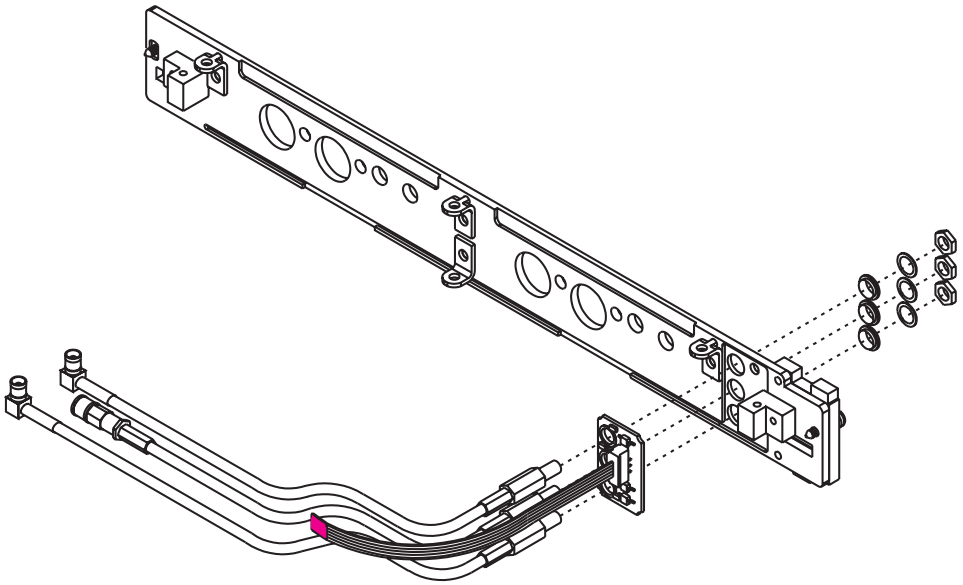
3 Using a 9/16" nut driver, remove the four nuts and washers from the BNCs as shown.



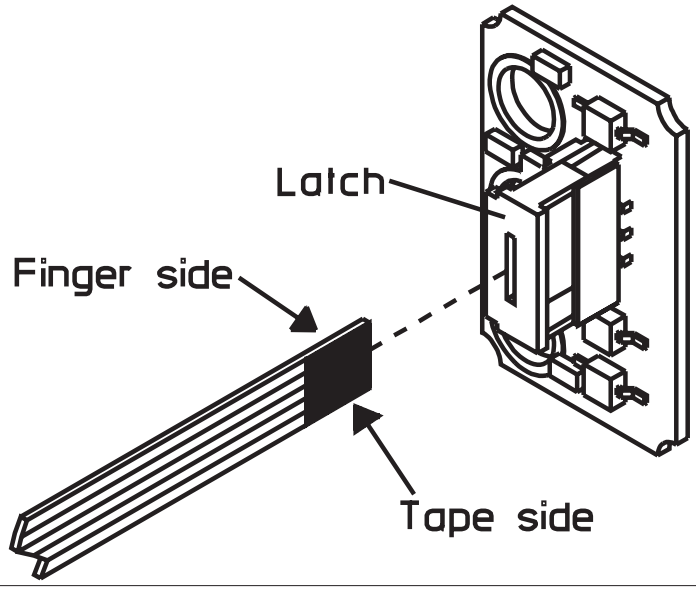
4 Using a T-8 Torx driver, remove the screw that attaches the front panel to the bottom cover. Gently pull the front panel off.



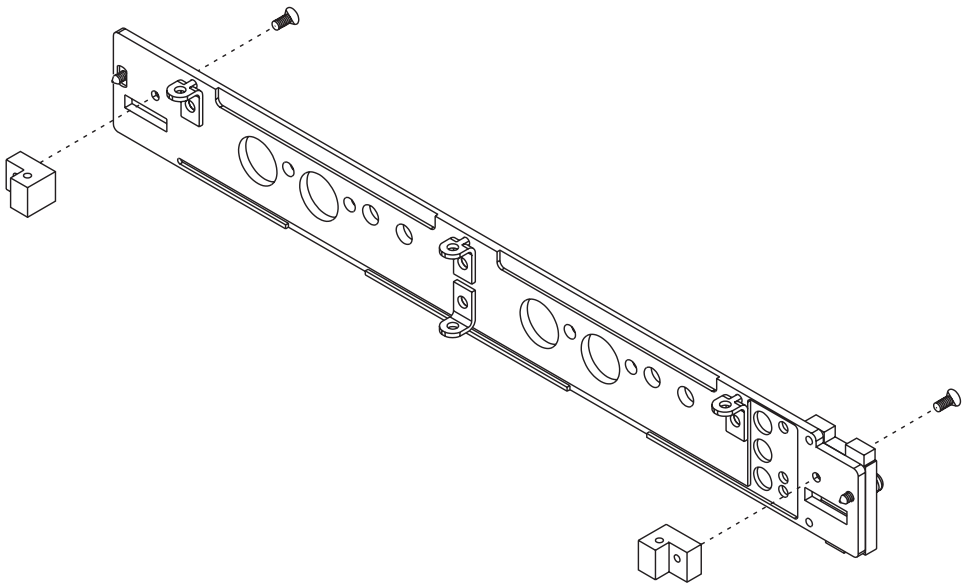
5 Remove the nuts that fasten the cables and assembly to the front panel. Using a 1/4-inch nut driver.



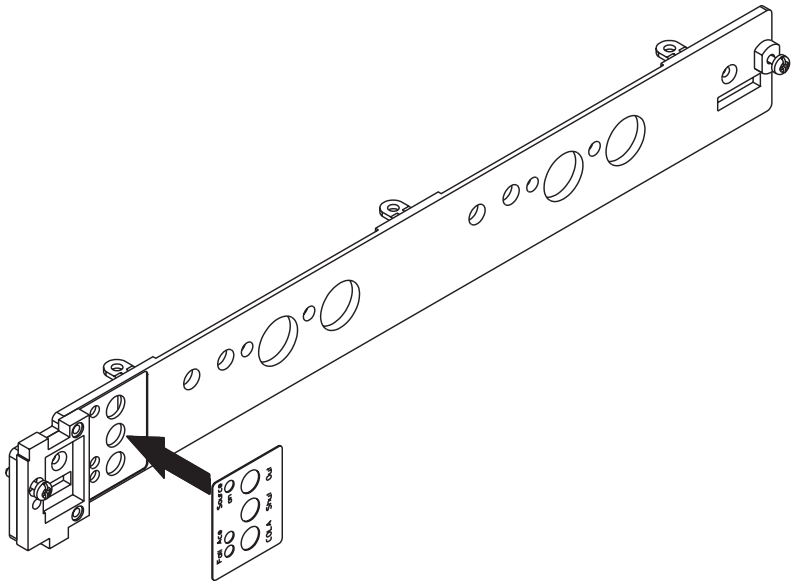
6 Remove ribbon cable from the A4 assembly, by pulling back the latch on the connector and and removing cable. Be sure to note the orientation of the cable.



7 To replace the front panel with another that does not have its own side brackets, remove the brackets from the old front panel using a T-8 Ttorx driver. Be sure to note the positioning of the brackets, alignment is critical.



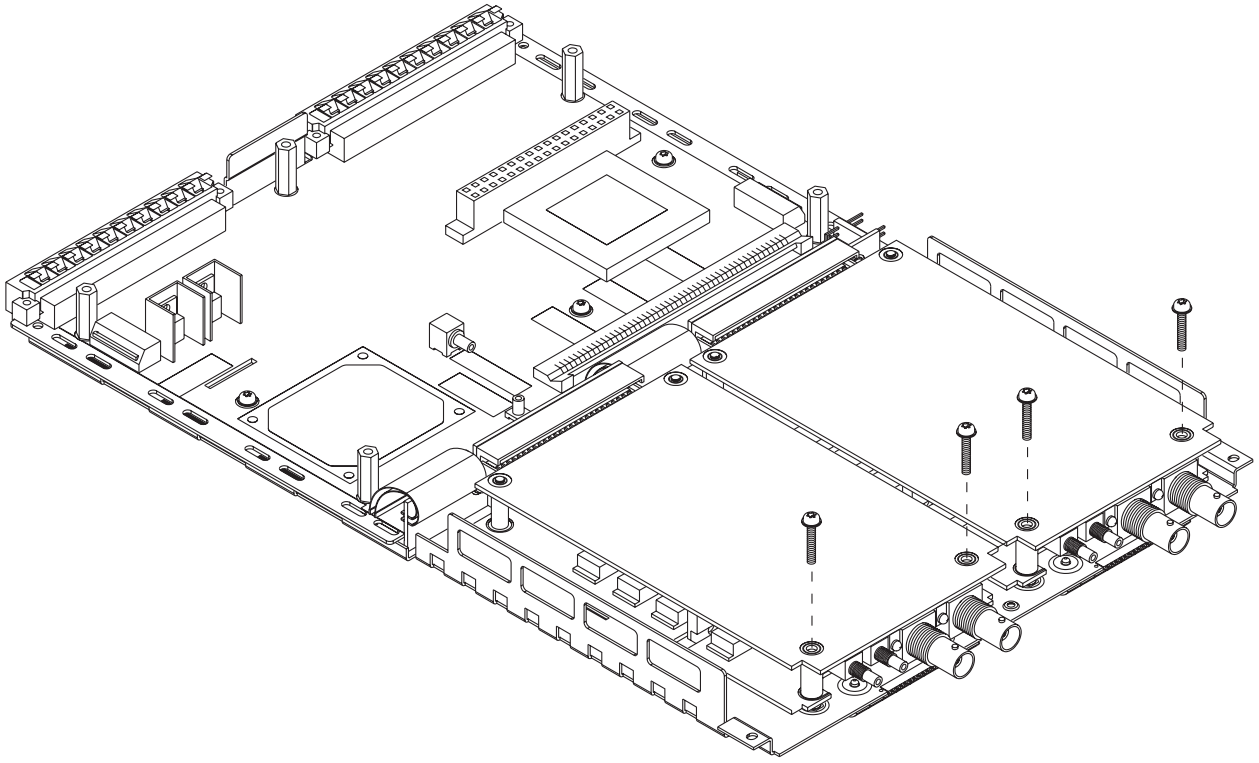
8 To replace the front panel with another that does not have the label already attached, remove the tape backing and place it on the front panel as shown.



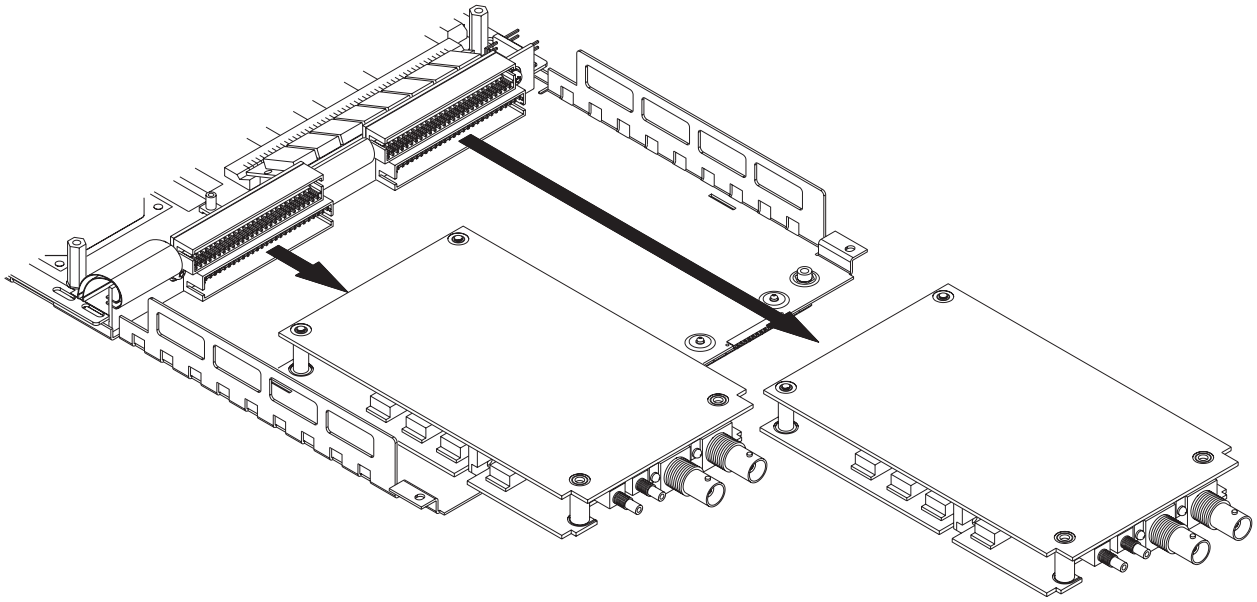
To remove the source SCA assemblies

1 Remove top cover, see “To remove the top cover.” Remove the front panel, see steps 1 through 4 in “To remove the front panel.” Note that the following steps are showing illustrations of an VT1434A with a standard configuration (two two-channel source SCA assemblies). If the VT1434A has option 1DM (one two-channel source SCA assembly), the following steps will be the same except the quantity of screws and only one source SCA assembly.

2 Using a T-10 torx driver, remove the four screws that attach the assemblies to the bottom cover.

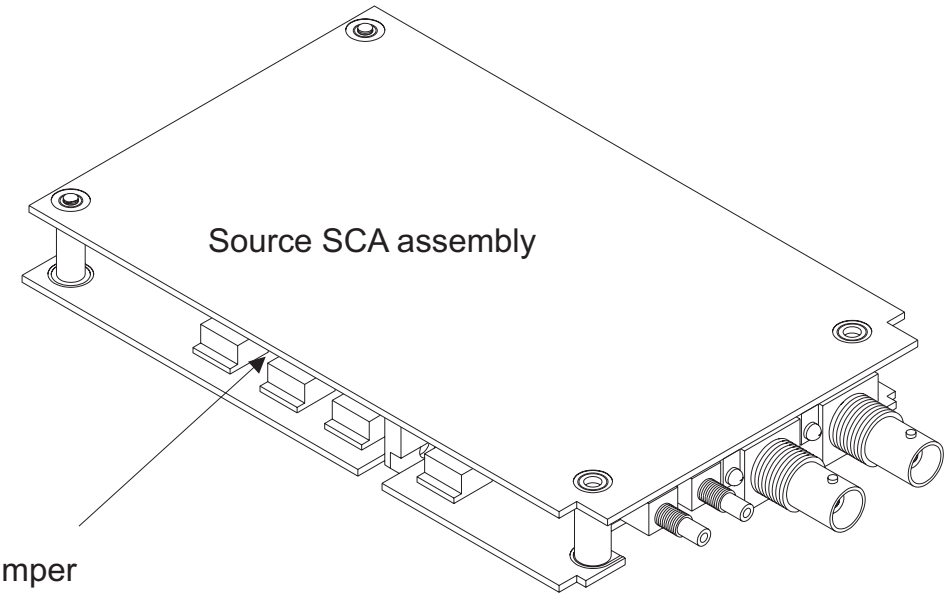


3 Remove the assembles by gently pulling them forward, releasing them from the connectors.



To locate the source boot jumper

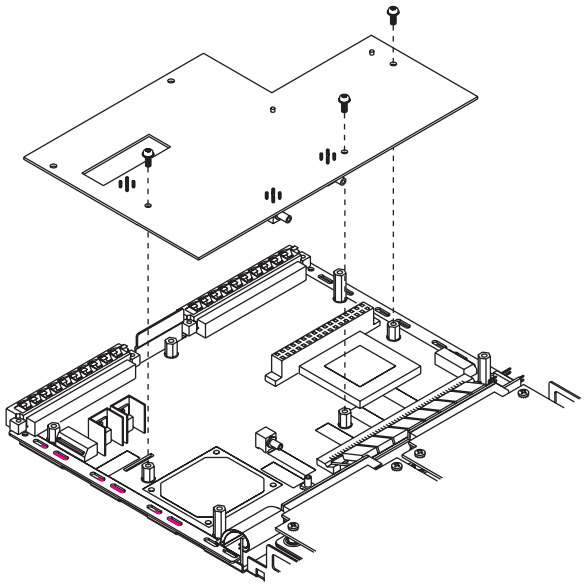
1 If performing the VT1432A Arb Source ROM Recovery Service Procedure, locate the source board boot jumper as shown in the illustration below. Separate the two boards of the source SCA assembly to access the jumper. See the file /opt/e1342/arbsrc/romfix.txt for more information about this procedure.



To remove the option 1D4 assembly

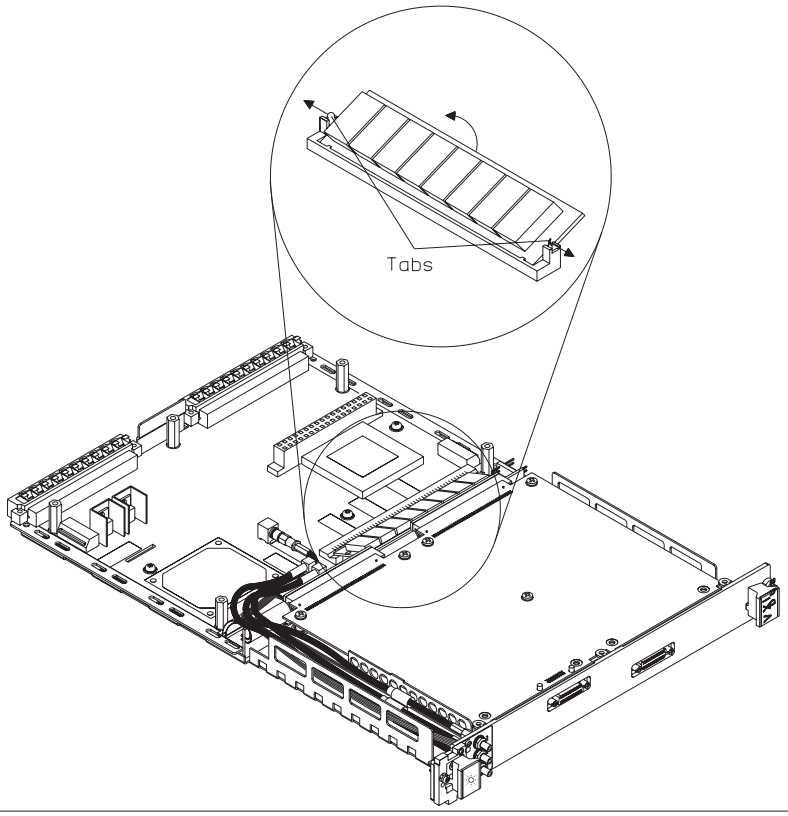
1 Remove the top cover, see “To remove the top cover.” Disconnect the three cables leading to the A41 assembly and move cables aside.

2 Using a T-10 Torx driver, remove the three screws that attach the assembly to the VT1434A and lift the assembly off.



To remove the A22/A24 assembly

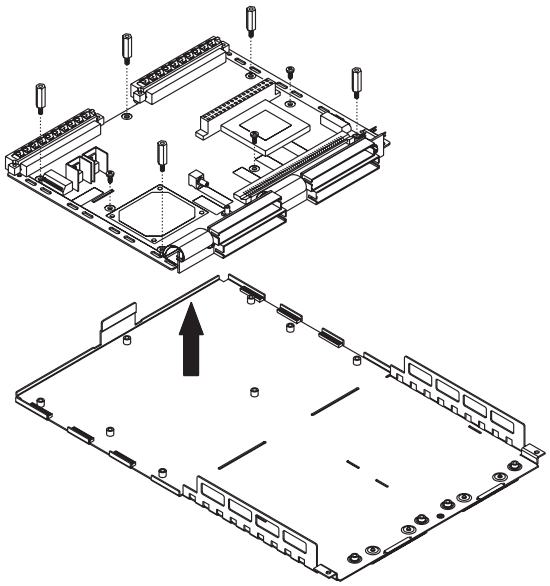
1 Remove the top cover, see “To remove the top cover.” Gently push the silver tabs outward and tilt the A22/A24 assembly forward releasing it from the connector.



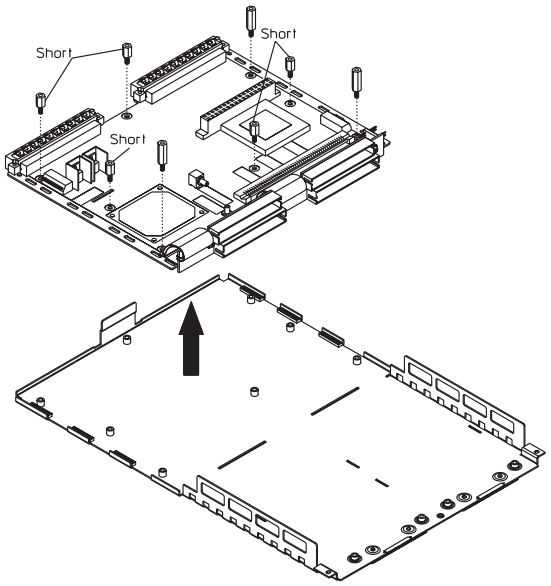
To remove the A10/A11 assembly

1 Remove top cover and input assemblies. See “To remove the top cover,” and “To remove the input assemblies.”

2A *If the module does NOT have option 1D4 do the following:* Remove the five standoffs using a 1/4-inch nut driver and remove the three screws using a T-8 Torx driver.



2B *If the module has option 1D4 do the following:* Remove the 1D4 option assembly, see "To remove the option 1D4 assembly." Remove the three long and the five short standoffs using a 1/4-inch nut driver.



8

Backdating

Backdating

This chapter documents modules that differ from those currently being produced. With the information provided in this chapter, this guide can be modified so that it applies to any earlier version or configuration of the module.

Appendix A

Register Definitions

The VT1434A VXI Registers

The VT1434A 4-Channel 65 kSamples/s Arbitrary Source is a register-based VXI device. Unlike message-based devices which use higher-level programming using ASCII characters, register-based devices are programmed at a very low level using binary information. The greatest advantage of this is speed. Register-based devices communicate at the level of direct hardware manipulation and this can lead to much greater system throughput.

Users do not need to access the registers in order to use the VT1434A. The VT1434A's functions can be more easily accessed using the VT1434A Host Interface Library software. However this chapter describing the registers is provided as supplementary information.

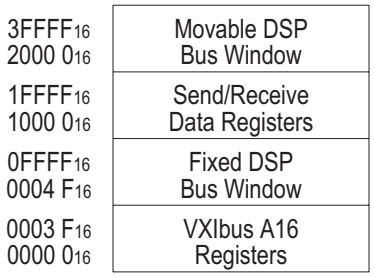
The A16 Registers

The following A16 registers are accessible at the base address defined by the device's logical address. The register at offsets 00_{16} to E_{16} are not accessible using longword (D32) accesses. The registers at offsets 10_{16} to $3E_{16}$ may be accessed by any of the D08(EO), D16 or D32 modes. All of these registers are also accessible at the device A24 base address.

Address	Read	Write
$3E_{16}$	Parameter 7 Register	
$3C_{16}$		
$3A_{16}$	Parameter 6 Register	
38_{16}		
36_{16}	Parameter 5 Register	
34_{16}		
32_{16}	Parameter 4 Register	
30_{16}		
$2E_{16}$	Parameter 3 Register	
$2C_{16}$		
$2A_{16}$	Parameter 2 Register	
28_{16}		
26_{16}	Parameter 1 Register	
24_{16}		
22_{16}	Query Response Register	Command Register
20_{16}		
$1E_{16}$		
$1C_{16}$		
$1A_{16}$	Send Data	
18_{16}		
16_{16}	RAM 1	
14_{16}		
12_{16}	RAM 0	
10_{16}		
$0E_{16}$	IRQ Status Register	IRQ Reset Register
$0C_{16}$	IRQ Config Register	
$0A_{16}$	Page Map Register	
08_{16}	Port Control Register	
06_{16}	Offset Register	
04_{16}	Status Register	Control Register
02_{16}	Device Type	
00_{16}	ID Register	Logical Address Register

The A24 Registers

The following A24 registers are accessible at the base address defined by the device's offset Register. The registers at offsets 0 to E_{16} are not accessible using longword (D32) accesses. The registers at offsets 10_{16} to $3FFFF_{16}$ may be accessed by any of the of the D08(EO), D16 or D32 modes.



The A24 registers are defined as follows:

- VXIbus A16 Registers: These are the same registers accessed at the device's A16 base address.
- Fixed DSP Bus Window: Accesses to this region are mapped to the corresponding locations at the base of the internal DSP's memory map, also accessible through Page 0 of the moveable DSP bus window.
- Send/Receive Data Registers: Accesses to any address in this region will read/write the Send and Receive Data registers defined in the A16 register set. VMEbus D32 Block Transfers are supported for these addresses only.
- Movable DSP Bus Window: Accesses to this region are mapped (by the Page Map register) to different 128 kB regions of the internal DSP bus.

The VXIbus Registers are defined as follows:

- Id Register: A read of this 16 bit register provides information about the device's configuration. Its value is always CFFF16 as defined in the following table.

Bit	15-14	13-12	11-0
Contents	11 (Register Based Device)	00 (A16/A24)	111111111111 (Agilent's ID)

- Logical Address Register: A write to this register changes the device's logical address according to the VXIbus Dynamic Configuration protocol. Its format is defined in the following table.

Bit	15-8	7-0
Contents	No effect	Logical Address

- Device Type Register: A read of this register provides information about the device's configuration. Its format is defined in the following table.

Bit	15-12	11-0
Contents	0101 (256k of A24)	Model Code (203_{16} for VT1434A)

- Status Register: A read of this register provides information about the device's status as defined in the following table.

Bit	15	14	13-12	11	10	9	8
Contents	A24 Active	MODID*	Unused	Block Ready	Data Ready	ST Done	Loaded

Bit	7	6	5	4	3	2	1	0
Contents	Done	Err*	Unused	HW OK	Ready	Passed	Q Resp Ready	Cmd Ready

A24 Active: A one (1) in this field indicates that the A24 registers can be accessed. It reflects the state of the Control register's A24 Enable bit.

MODID*: A one (1) in this field indicates that the device is not selected via the P2 MODID line. A zero (0) indicates that the device is selected by a high state on the P2 MODID line.

Unused: A read of these bits will always return zero (0).

Block Ready: A one (1) indicates that there is a block of data available to be read from the Send Data registers. A zero (0) indicates that less than a full block is available.

Data Ready: A one (1) indicates that there is at least one word (32 bits) of data available in the Send Data register. A zero (0) indicates that there is not valid data in the Send Data register.

ST Done: A one (1) indicates that the internal DSP has competed and passed its self test.

Loaded: A one (1) indicates that the internal DSP has successfully booted and has loaded a valid model code.

Done: A zero (0) indicates that the on-card microprocessor has not finished processing the last command and the Err* bit is not valid. This bit is set and cleared by the DSP.

Err*: A zero (0) indicates that an error has occurred in communicating with the DSP (for example: invalid parameters). This bit is set and cleared by the DSP.

Ready: The meaning of this depends on the state of the Passed bit. While Passed is false, a one(1) indicates that the device is in the Config Reg Init state and the Model Code bits of the Device Type register are not valid, while a zero (0) indicates that the device is in either the self test or failed state. When Passed is true, a one (1) indicates that the DSP has finished its initialization and is ready for normal operation, while a zero (0) indicates that the device is in the passed state.

Passed: A zero (0) indicates that the device is in either the Hard Reset, Soft Reset, Config Reg Init, Failed or Init Failed state. A one (1) indicates that the device is in the passed state.

HW OK: A one (1) indicates that all the on-card FPGAs have successfully be initialized.

Q Resp Ready (Query Response Ready): A one (1) indicates that the Query Response Register is loaded and ready to be read. It is set by the DSP and cleared in hardware by a write to the Command Register.

Cmd Ready: A one (1) indicates that the command register and parameter register are available for writing. It is set by the DSP microprocessor and cleared in hardware by a write to the Command Register. This bit, when zero (0) additionally indicates that the Done bit is not valid.

- Control Register: A write to this register causes specific actions to be executed by the device. The actions are described in the following table.

Bit	15	14-2	1	0
Contents	A24/A32 Enable	Unused	Sysfail Inhibit	Reset

A24/A32 Enable: A one (1) in this field enables access to the device's A24 VMEbus registers. A zero (0) disables such access.

Sysfail Inhibit: A one (1) disables the device from driving the SYSFAIL* line.

Reset: A one (1) forces the device into a reset state.

- Offset Register: This read/write register defines the base address of the device's A24 registers. The four most significant bits of the Offset register are the values of the four most significant bits of the device's A24 register addresses. The 12 least significant bits of the Offset register are always zero (0). Thus, the Offset register bits 15-12 map the VMEbus address lines A23-A20 for A24 register accesses. A read of the Offset register always returns the address offset most recently written to the Offset register.
- Port Control Register: This register is used to override the Local Bus control of the device. (This applies to VT1434A modules that are equipped to use Local Bus). It has the following format:

Bit	15-2	1	0
Contents	Unused	LBus Pipe	LBus Enable

LBus Pipe: Writing a one (1) puts the Local Bus into pipeline mode, if the LBus Enable bit is also set. Writing a zero (0) allows the Local Bus to operate in some other mode.

LBus Enable: Writing a one (1) enables the Local Bus interface. Writing a zero (0) disables the local bus interface. RESET VALUE: 0

- Page Map Register: This read/write register defines the internal location of the movable window into the device's DSP bus. (This 512 kB window begins at 512 kB into the device's A24 registers.) The eight least significant bits of the Page Map register are the page number. These bits are mapped to the internal DSP bus address lines as follows:

  Bit 0: DSP A(17)
  Bit 1: DSP A(18)
  Bit 2: DSP A(19)
  Bit 3: DSP A(20)
  Bit 4: DSP A(21)
  Bit 5: DSP A(22)
  Bit 6: DSP A(30) and A(24)
  Bit 7: DSP A(31)

The eight most significant bits of the Page Map Register are always zero (0).

- IRQ Config Register: This register configures the first VMEbus interrupt source. It provides for selection of the VMEbus IRQ level used and a bit mask. It has the following format:

Bit	15-8	7-4	3	2-0
Contents	Mask	Unused	IRQ Enabled	IRQ Line

Mask: This is a bit mask used to enable up to eight interrupt causes. A bit value of zero (0) disables the corresponding interrupt source. RESET VALUE: 0

IRQ Enable: A one (1) in this bit enables the generation of IRQ's. A zero (0) resets each of the eight interrupt causes and status bits. RESET VALUE: 0

IRQ Line: This field select which VMEbus IRQ line is driven by this device. A value of zero (0) disconnect the interrupt source. RESET VALUE: 0

- IRQ Status Register: This read-only register indicates the reason for asserting the VMEbus interrupt. The format of the data is identical to that of the Status/ID word returned by an interrupt acknowledge (IACK) cycle. It differs from the IACK cycle in that the IACK cycle will clear the status bits and cause the de-assertion of the IRQ line. The register has the following format:

Bit	15-8	7-0
Contents	Status	Logical Address

Status: Each of these bits indicates the status of a cause of interrupt. A one (1) in a bit position indicates that the corresponding source is actively requesting and interrupt.

Logical Address: This is the device's current logical address.

- IRQ Reset Register: This register is used to resent the interrupt function. It has the following format:

Bit	15-8	7-0
Contents	Reset Bits	Unused

Reset Bits: Writing a one (1) to any of these bits will clear the corresponding bit in the IRQ status register . This will not disable subsequent interrupt generation. Clearing all of the IRQ status bits will cause the de-assertion of the IRQ line. Writing a zero (0) has no effect.

- Ram 0-1: These are 32-bit general purpose RAM locations which are also accessible to the on-board DSP. See the following section regarding D16/D08 access of 32-bit registers.
- Send Data Register: Reading this register gets the next available word from the measurement data FIFO. The measurement data FIFO is a 32-bit device. See the following section regarding D16/D08 access of 32-bit registers.
- Receive Data Register: Writing to this register puts a word into the source data FIFO. The source data FIFO is a 32-bit device. See the following section regarding D16/D08 access of 32-bit registers.
- Count Register: The Count register contains an unsigned 16-bit integer which is the number of 16-bit words of data which are currently available from the Send Data register or which the Receive Data register is currently ready to accept. While a device is generating or accepting data, the Count register may indicate fewer than the actual number of words available.
- Query Response/Command Register: This register is used to send commands to and receive responses from the device. It is implemented as a 32-bit RAM location. Writing the least significant byte (highest address) clears the Command/Parameter Ready and Query Response Ready bits in the status register and interrupts the on-board DSP. See the following section regarding D16/D08 access of 32-bit registers and the communication protocol.

- Parameter 1-7 Registers: These are 32-bit RAM locations used to pass parameters along with commands to the device or query responses from the device. See the following section regarding D16/D08 access of 32-bit registers and the communication protocol.

32-bit Registers

Several of the A16 registers (and all other 24-bit registers) are implemented as 32-bit-only resources. These are accessible using VMEbus D16 and D08(EO) accesses. However certain restrictions apply. The affected A16 registers are:

- RAM 0-1
- Send Data
- Receive Data
- Query Response Command
- Parameter 1-7

Reading 32-bit Registers

When reading a 32-bit register using 8- or 16-bit modes, a simple caching mechanism is used. On any read including the most significant byte (lowest address), the 32-bit register is read and all 32-bits are latched into the read cache. A read not including the most significant byte fetches data from the read cache, without re-reading the register. This insures that the data will be unchanged by any intervening write by the DSP (which would result in garbled data).

This mechanism also introduces a hazard. Reads of less significant bytes get data from the 32-bit register last read by a most-significant-byte read. In other words, the least significant byte can’t be read first or by itself. Thus there are two important rules:

1 Always read all 32 bits of a 32-bit register.
2 Always read the most significant part first.

Writing 32-bit Registers

When writing to a 32-bit register using 8- or 16-bit modes, a simple caching scheme is also employed. On any write not including the least significant byte (highest address), the data is latched into the write cache. A write to the least significant byte causes the cached data to be written to the 32-bit register (in parallel with the current data for the least significant bytes(s).

This mechanism has its own hazards. Writes to the least significant byte will always include the most recently cashed data, whether intended for that register or not. Lone writes to the most significant part of a 32-bit register will be lost if not followed by a write to the least significant part of the same register. Thus there are two important rules:

1 Always write all 32 bits of a 32-bit register.
2 Always write the least significant part last.

Command/Response Protocol

The Command/Response protocol uses the following resources:

- Command/Query Response register implemented as a general purpose RAM
- Three parameter registers implemented as a general purpose RAM
- Additional A24 accessible RAM contiguous with the parameter registers
- The Command Ready, Query Response Ready, Err* and Done bits of the Status register.

The RAM registers are the communications media, while the Status register bits provide synchronization. In general, a controller sends a command to the DSP by first writing any parameters to the parameter registers and the following RAM location. It then writes the command to the command register, which clears the Command/Parameter Ready bit and interrupts the DSP. At this point, the DSP has exclusive access to the RAM registers. The controller may not access that RAM again until the Command/Parameter Ready bit is true.

When interrupted, the DSP reads the command and its parameters, writes any response data back to the Query Response Register and any other data to the parameter registers and the following RAM and set the Command/Parameter Ready bit true.

The Query Response Ready bit is used to indicate that the DSP has written query data to the RAM registers. It is set by the software and cleared by a write of the Command Register.

The Done bit is set by DSP software when it finishes execution of a command or a command sequence. This may by long after it has set the Command/Parameter Ready bit. The DSP software clears the Done bit immediately on receipt of a new command, before it sets the Command/Parameter Ready bit.

The Err* bit is asserted (to 0) by the DSP software to indicate an error in the decoding or execution of a command. It is asserted (to 1) if the command was executed with no error. This bit must be valid before Done is set at the end of a command.

In order to avoid contention and/or invalid data reads, there are certain rules that must be observed:

1. A controller must not write to any of the RAM registers when Command/Parameter Ready is false.
2. The DSP must not write to any of the RAM registers when either Command/Parameter Ready or Query Response Ready is true.
3. A controller must not read any of the RAM registers when Query Response Ready is false.
4. The DSP must not read any of the RAM registers when Command/Parameter Ready is true.
5. When writing a command together with parameter, a controller must always write to the Command Register last.
6. When executing a command that requires it to return response data, the DSP must set the Query Response Ready bit no later than the Command/Parameter Ready bit.
7. The DSP must not clear the Done bit while Command/Parameter Ready is true.
8. The DSP must not change the Err* bit while Done is true.
9. A controller must not regard the done bits a valid while Command/Parameter Ready is false.
10. A controller must not regard the Err* bit as valid while Done is false.

Controller Protocol Examples

There are three basic procedures used by a controller, Write Command, Read Response and Wait for Done. These can be combined for more complex sequences.

Write Command

This is the procedure to send a command to the DSP.

1. Wait for Command/Parameter Ready true.
2. Write any parameters to the Parameter registers and RAM.
3. Write the command to the Command register.

Read Response

This is the procedure for reading a response to query command.

1. Wait for Query Response Ready true.
2. Read the data from the Query Response register and any additional data from the Parameter registers and RAM.

Wait for Done

This is the procedure to wait for command completion and check for error.

1. Wait for Command/Parameter Ready true.
2. Wait for Done true.
3. If Err* = 0 , handle error.

Complex Sequences

A robust procedure for sending a query and reading the response would look like this:

1. Send Command.
2. Wait for Done.
3. If no error then Read Response.

Multiple commands may be sent with a test for errors at the end of the sequence. This example sends three commands before checking for errors.

1. Send Command.
2. Send Command.
3. Send Command.
4. Wait for Done.

DSP Protocol

When a controller writes to the Command register, a DSP interrupt is generated. When responding to this interrupt, the DSP will follow this procedure.

1. Clear the Done bit.
2. Read and decode the command from the Command register.
3. Read any parameters from the Parameter registers and RAM.
4. If a response data is required:
   a Write the data to the Query Response register, Parameter registers and RAM.
   b Set Query Response Ready true.
5. Set Command/Parameter Ready true.
6. Finish command execution.
7. If any errors are pending set Err* = 0, else set Err* = 1.
8. Set Done true.

There are two additional requirement for the DSP:

1. Once it begins processing a command interrupt, the DSP must defer processing subsequent commands until it has finished.
2. The DSP software maintains an error(s) pending flag (and possibly and error queue) that is set by any command decoding or execution error and cleared by some other method such as an error query.

DSP Bus Registers

There are two 32-bit registers in the DSP bus address space. The VXI FPGA does not assert TA* when these registers are accessed.

$200A_{16}$	DSP Command Register
$200B_{16}$	Boot Register

Note that these registers appear multiple times in the memory map, since only the address lines A31-30, A17-13, A9-8 and A3-0 are used for decoding.

The A24 registers are defined as follows:

- Boot Register: This read/write register is used to configure the device after a device reset. It has the following format:

Bit	31-16	15	14	13	12	11-0
Contents	Unused	Spare	ST Done	Loaded	Ready	Model Code

Spare: This read/write bit has no pre-defined function.

ST Done: This bit should be written to a one (1) when the DSP successfully competes its self-test, within five seconds after SYSRESET* is de-asserted. Its initial value is zero (0).

Loaded: This bit should be written to a one (1) when (or immediately after) the DSP loads the model code, before competing its self-test. Its initial value is zero (0).

Ready: This bit is written to a one (1) to indicate that the device is ready for normal operation. Its initial value is zero (0).

Model Code: As soon as possible and within 25 ms after coming out of reset, when the DSP has valid code loaded, it should write the VXI model code to these bits. Their initial value is 0x0200.

- DSP Command Register: This register is used to assert VXI interrupts and toggle various status register bits. Many of the bits in this register are grouped into related Clock and Value pairs. This allow the bits to be modified independently with single register writes. In order to change an output value, the Clock bit must be written as a one (1), while the Value is written as the desired output value. Writing the Clock bit as a zero (0) will not change the output state. The current state is read from the Value bit.

The DSP Command register has the following format:

Bit	31-24	23	22	21	20	19	18	17	16
Contents	Unused	FIFO Enable Clock	FIFO Enable Value	FIFO In Clock	FIFO In Value	DONE Clock	DONE Value	ERRn Clock	ERRn Value

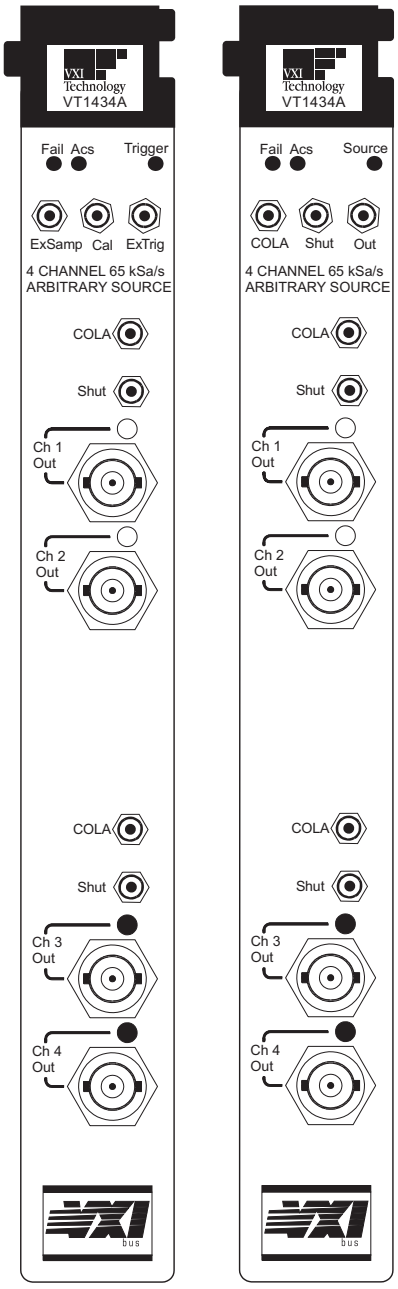
Bit	15	14	13	12	11	10	9-8	7-0
Contents	Q Resp Ready Clock	Q Resp Ready Value	Cmd Ready Clock	Cmd Ready Value	IRQ Enable Clock	IRQ Enable Value	Unused	IRQ7-0

VT1434A

Technical Specifications

4-Channel 25.6 kHz Arbitrary Source

Rev. November 2003



VT1434A

VT1434A with additional Arbitary Source Option 1D4

The VT1434A 4-Channel 65 kSamples/s Arbitrary Source is a C-sized VXI module. It provides a maximum signal data rate of 65,536 samples per second, per channel.

The VT1434A may contain one or two 2-channel source assemblies so that the module may have a total of up to four outputs. In addition, if option 1D4 is installed, it provides one additional output for a total of five output channels.

This intelligent module provides arbitrary waveform output capability with both loop mode and continuous arbitrary waveforms, using dynamic updating of data.

Specifications

General

Output Modes	Sine, burst sine Pseudo random noise, with burst and band translation Arbitrary waveform with loop or continuous output and burst
Operating Modes	
16-Bit Mode	
Number of channels	2, 4 or 5
Maximum signal frequency	25.6 kHz
Output data rate (Fs)	48.00 kHz to 65.536 kHz
20-Bit Mode	
Number of channels	1 or 2, 3 with optional source
Maximum signal frequency	6.4 kHz
Output data rate (Fs)	12.00 kHz to 16.384 kHz
Frequency Accuracy	± 0.012% (120 ppm)

Signal Output

Number of Output Channels	2, 4 or 5, depending on option selected
Maximum Amplitude	10 V_P nominal
Output Impedance	< 0.5 Ω (typical)
Maximum Output Current	100 mA (typical)
Maximum Capacitive Load	0.01 μF (typical)
Amplitude Control (signal amplitude = amplitude range × *amplitude scale factor)*	
Maximum signal amplitude	10 V_P nominal
Amplitude ranges	10 V_P to 79 mVp in 0.375 dB steps
Amplitude scale factor	1.0 to 0.0, with 16-bit or 20-bit resolution
Residual Output Noise Voltage 1 Vp Range, Freq > 500 Hz	< 500 nV/$\sqrt{Hz}$
Residual DC Offset	
Offset after autozero	± 2 mV
Offset after shutdown	± 20 mV
Channel-to-channel Crosstalk *(at sine frequency of generating channels, all channels same range)*	
Signal amplitude ≥ 1.0 Vp	< - 80 dB
Signal amplitude < 1.0 Vp	< - 80 dB V_P (100 μV_P)
Output Overload Trip	> 17 V (typical)
Amplitude Ramp-down Time (programmable)	0 to 30 seconds
Shutdown	
Shutdown input signal	TTL levels
Shutdown time	< 5 s
Shutdown time, ac fail	< 4 ms

Sine Output Mode

Sine Frequency (65.536 kHz Fs)	
Frequency range	0 to 25.6 kHz
Frequency resolution	
Sine frequency ≤ 1 kHz	244 μHz
1 kHz<sine frequency ≤ 10 kHz	2.384 mHz
10 kHz < sine frequency ≤ 25.6 kHz	6.10 mHz
Amplitude Accuracy (1 kHz sine wave, ≥ *200 Ω load)*	
10 Vp to 0.158 V_P ranges	± 0.20 dB (2.3 %)
0.152 V_P to 79 mV_P ranges	± 0.40 dB (4.7 %)
Flatness (relative to 1 kHz)	± 0.5 dB
Harmonic and Aliased-harmonic Distortion (≥ 1 kΩ load)	
1 V_P range, 1.0 scale factor, 0 to 6.4 kHz (20 bit mode)	< - 80 dBc
2 to 10 Vp range, 0.05 to 1.0 scale factor, 0 to 25.6 kHz (16-bit mode)	< - 70 dBc
Spurious Responses	<- 60 dBV_P
Channel-to-channel Phase Match at 1 kHz	± 1.0 deg

Noise Output Modes

Frequency Spans	see table: Noise/Arb Frequency Spans
Passband Flatness *(Measurement BW > 1% of span)*	< 1.2 dB (typical)
Crest Factor	4.1 (typical)
Percent In-band Energy	> 90% (typical)

Frequency Band Translation (Zoom)
(16 and 20 bit modes):

For Fs=	Maximum Span	Maximum Center Frequency
65,536 kHz (channels 1 and 3 active, only)	5.12 kHz	5.12 kHz
64,000 kHz (channels 1 and 3 active, only)	5.00 kHz	5.00 kHz
51,200 kHz	4.00 kHz	4.00 kHz
48,000 kHz	3.750 kHz	3.750 kHz
40.96 kHz	2.200 kHz	2.200 kHz

Minimum span: Maximum Span ÷ 2^{16}

Center frequency settibility:	
Sine frequency ≤ 1 kHz	244 0 μHz
1 kHz<sine frequency ≤ 5 kHz	1.22 mHz

Mode	Sample Rate (Hz)	Bandwidth (Hz)
16-bit	65536	25600
16-bit	64000	25000
16-bit	51200	20000
16-bit	48000	18750
16-bit	40960	16000
16-bit	32768	12800
16-bit	32000	12500
16-bit	25600	10000
16-bit	24000	9375
16-bit	20480	8000
16.20-bit	16384	6400
16.20-bit	16000	6250
16.20-bit.zoom	13107.2	5120
16.20-bit.zoom	12800	5000
16.20-bit	12000	4687.5
16.20-bit.zoom	10240	4000
16.20-bit.zoom	9600	3750
16.20-bit.zoom	8192	3200
16.20-bit	8000	3125
16.20-bit.zoom	6553.6	2560
16.20-bit.zoom	6400	2500
16.20-bit	6000	2343.75
16.20-bit.zoom	5120	2000
16.20-bit.zoom	4800	1875
16.20-bit.zoom	4096	1600
16.20-bit	4000	1562.5
16.20-bit.zoom	3276.8	1280
16.20-bit.zoom	3200	1250
16.20-bit	3000	1171.875
16.20-bit.zoom	2560	1000
16.20-bit.zoom	2400	937.5
16.20-bit.zoom	2048	800
16.20-bit	2000	781.25
16.20-bit.zoom	1638.4	640
16.20-bit.zoom	1600	625
16.20-bit	1500	585.9375
16.20-bit.zoom	1280	500
16.20-bit.zoom	1200	468.75
16.20-bit.zoom	1024	400
16.20-bit	1000	390.625
16.20-bit.zoom	819.2	320
16.20-bit.zoom	800	312.5
16.20-bit	750	292.9688
16.20-bit.zoom	640	250
16.20-bit.zoom	600	234.375
16.20-bit.zoom	512	200
16.20-bit	500	195.3125
16.20-bit.zoom	409.6	160
16.20-bit.zoom	400	156.25
16.20-bit	375	146.4844
16.20-bit.zoom	320	125
16.20-bit.zoom	300	117.1875
16.20-bit.zoom	256	100
16.20-bit	250	97.65625
16.20-bit.zoom	204.8	80
16.20-bit.zoom	200	78.125
16.20-bit	187.5	73.24219
16.20-bit.zoom	160	62.5
16.20-bit.zoom	150	58.59375
16.20-bit.zoom	128	50
16.20-bit	125	48.82813
16.20-bit.zoom	102.4	40
16.20-bit.zoom	100	39.0625
16.20-bit	93.75	36.62109
16.20-bit.zoom	80	31.25
16.20-bit.zoom	75	29.29688
16.20-bit.zoom	64	25
16.20-bit	62.5	24.41406
16.20-bit.zoom	51.2	20
16.20-bit.zoom	50	19.53125
16.20-bit	46.875	18.31055
16.20-bit.zoom	40	15.625
16.20-bit.zoom	37.5	14.64844
16.20-bit	32	12.5
16.20-bit	31.25	12.20703
16.20-bit.zoom	25.6	10
16.20-bit.zoom	25	9.765625
16.20-bit	23.4375	9.155273
16.20-bit.zoom	20	7.8125
16.20-bit.zoom	18.75	7.324219
16.20-bit.zoom	16	6.25
16.20-bit	15.625	6.103516
16.20-bit.zoom	12.8	5
16,20-bit,zoom	12.5	4.882813

Noise/Arb Frequency Spans

Mode	Sample Rate (Hz)	Bandwidth (Hz)
16.20-bit	11.71875	4.577637
16.20-bit.zoom	10	3.90625
16.20-bit.zoom	9.375	3.662109
16.20-bit.zoom	8	3.125
16.20-bit	7.8125	3.051758
16.20-bit.zoom	6.4	2.5
16.20-bit.zoom	6.25	2.441406
16.20-bit	5.859375	2.288818
16.20-bit.zoom	5	1.953125
16.20-bit.zoom	4.6875	1.831055
16.20-bit.zoom	4	1.5625
16.20-bit	3.90625	1.525879
16.20-bit.zoom	3.2	1.25
16.20-bit.zoom	3.125	1.220703
16.20-bit	2.929688	1.144409
16.20-bit.zoom	2.5	0.976563
16.20-bit.zoom	2.34375	0.915527
16.20-bit.zoom	2	0.78125
16.20-bit	1.953125	0.762939
16.20-bit.zoom	1.6	0.625
16.20-bit.zoom	1.5625	0.610352
16.20-bit	1.464844	0.572205
16.20-bit.zoom	1.25	0.488281
16.20-bit.zoom	1.171875	0.457764
16.20-bit.zoom	1	0.390625
16.20-bit	0.976563	0.38147
16.20-bit.zoom	0.8	0.3125
16.20-bit.zoom	0.78125	0.305176
16.20-bit	0.732422	0.286102
16.20-bit.zoom	0.625	0.244141
16.20-bit.zoom	0.585938	0.228882
16.20-bit.zoom	0.5	0.195313
16.20-bit	0.488281	0.190735
16.20-bit.zoom	0.4	0.15625
16.20-bit.zoom	0.390625	0.152588
16.20-bit	0.366211	0.143051
16.20-bit.zoom	0.3125	0.12207
16.20-bit.zoom	0.292969	0.114441
16.20-bit.zoom	0.25	0.097656
16.20-bit	0.244141	0.095367
16.20-bit.zoom	0.2	0.078125
16.20-bit.zoom	0.195313	0.076294
16.20-bit	0.183105	0.071526
16.20-bit.zoom	0.15625	0.061035
16.20-bit.zoom	0.146484	0.05722
16,20-bit,zoom	0.125	0.048828

Arbitrary Output Mode	
Maximum signal bandwidth	25.6 kHz
Buffer size	40,960 samples x 2 buffers
Continuous Arb Data Rate	The Noise/Arb Frequency Spans table gives the continuous rate at which a user must supply data for a given span.

Constant Level Output	
Output Level at 1 kHz (after 1 second settling, amplitude scale factor is > 0.001)	1 V_P (nominal)
Output Impedance	1.2 kΩ (typical)
Flatness 25 Hz to 5 kH, amplitude scale factor 0.001 to 1.0 5 Hz to 20 kHz, amplitude scale factor 0.01 to 1.0 5 Hz to 20 kHz, amplitude scale factor 0.1 to 1.0	 1.13 Vp to 0.50 Vp (+10, -6.0 dB) (typical) 1.13 Vp to 0.44 Vp (+10, -7.0 dB) (typical) 1.13 Vp to 0.88 Vp (±1.0 dB) (typical)
Sine Wave Distortion (at 1 kHz, amplitude scale factor 0.1 to 1.0)	- 40 dBc (typical)
Residual DC Offset	< 5 mV (typical)

Summer Input (optional 5th channel only)	
Maximum Input Level	10 Vp
Gain, Summer Input to Signal Output	0 ± 0.5 dB at 1 kHz
Input Impedance	> 10 kΩ (typical)
Flatness, DC to 25.6 kHz	±0.5 dB (typical)
Sine Wave Distortion	- 80 dBc (typical)
Residual DC Offset	1 mV (typical)

Features

VXI Standard Information	Conforms to VXI revision 1.4 C-size, single slot width Register-based programming “Slave” Data Transfer Bus functionality A24 address capability D32 data capability Optional Local Bus capability SUMBUS driver and receiver Requires 2 or 4 TTLTRG_ lines for multi-module synchronization
Signal Processing	33 MHz Motorola 96002 DSP 2 banks of 128k word static RAM 128 kbytes Flash ROM Direct Memory Access (DMA) data transfer 4 Mbytes dynamic RAM with option ANM 32 Mbytes dynamic RAM with option ANC

Software Drivers

Driver Type	C libraries with source code
Supported Operating Systems	Microsoft Windows® 95 or later and Windows NT® and HP-UX 10.20
Supply Media	CD-ROM
VXI*plug&play* Compliance	C libraries support MS Windows 95 or later and Windows NT and HP-UX 10.20.

HP-UX 10.X for HP 9000 Series 700 and 800 computers are X/Open Company UNIX 93 branded products.

MS Windows is a U.S. registered trademark of Microsoft Corporation.

Windows NT is a U.S. registered trademark of the Microsoft Corporation.

General Characteristics

VXI Power Requirements	DC Current
No options installed	
+ 5 V	4.90 A
+ 12 V	0.60 A
– 12 V	0.55 A
+ 24 V	0.20 A
– 24 V	0.25 A
– 5.2 V	0.60 A
– 2 V	0.03 A
Source option installed (1D4)	
+ 5 V	0.60 A
+ 12 V	0.19 A
– 12 V	0.18 A
+24 V	0.03 A
– 24 V	0.03 A
– 5.2 V	0.00 A
– 2 V	0.00 A
Dynamic Current	
+ 5 V	0.03 A
+ 12 V	0.04 A
– 12 V	0.05 A
+24 V	0.01 A
– 24 V	0.01 A
– 5.2 V	0.03 A
– 2 V	0.01 A
VXI Cooling Requirements	4.39 liters/second 0.32 mm H_2O
Warm-up Time	15 minutes

Specification Note

Specifications describe warranted performance over the temperature range of 0° to 50°C, after a 15-minute warm-up from ambient conditions. Supplemental characteristics identified as “typical”, provide useful information by giving non-warranted performance parameters.
Typical performance is applicable from 20° to 30°C.

Abbreviations

Fs = sample rate of DAC.

Fc = cut off frequency of high pass or low pass filters.

dBfs = dB relative to full scale amplitude range.

dBc = dB relative to carrier amplitude.

Typical = typical, non-warranted, performance specification included to provide general product information.

For more information on VXI Technology test & measurement products, applications, services and for a current sales office listing, visit our web site, http://www.vxitech.com. Or, contact one of the following centers and ask for a test and measurement representative.

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Glossary

A16 registers
Address space using 16 address lines. The VXI definition gives each VXI module 64 bytes of A16 registers.

A24 registers
Address space using 24 address lines. VXI modules can configure how much A24 address space they use.

Agilent VEE
An Agilent program for graphical programming. See *VEE*.

arbitrary source
A signal source capable of producing an arbitrary waveform according to the way it is programmed.

arbitration bus
See DTB arbitration bus.

ASCII
American Standard Code for Information Interchange, a standard format for data or commands.

backplane
A set of lines that connects all the modules in a VXI system.

baseband
A band in the frequency spectrum that begins at zero. In contrast a zoomed band is centered on a specified center frequency.

block mode
A mode of data-collecting used in instruments such as the Agilent/HP E1431. The instrument stops taking data as soon as a block of data has been collected. Overlap block mode in the VT1432A and VT1433B can be configured to act exactly like block mode.

block size
The number of sample points in a block of data.

C-Library (interface library)
A library of functions, written in C language, which can be used to operate the VT1432A and VT1433B.

C-size

One of several possible sizes for VXI modules. The VT1432A and VT1433B are C-size modules.

channel-dependent commands

Commands that are channel-dependent change a parameter for each channel independently.

COLA

Constant Output Level Amplifier.

continuous mode

A mode of data-collecting used in the VT1432A, the VT1433B and in other instruments such as the Agilent/HP E1431A. The instrument collects data continuously and stops only if the FIFO overflows.

D32, D16 and D08 (EO)

The VXI Bus provides 32 data lines. Modules can use all 32 lines or 16 lines or 8 lines. For example, “D16 access” refers to data read across 16 lines.

daisy-chain

A set of instruments or modules connected together in a line. Data and instructions enter each one before being buffered and passed out to the next module in line.

decimation filter

A digital filter that simultaneously decreases the bandwidth of the signal and decreases the sample rate. The digital filter provides alias protection and increases frequency resolution. For more information, see *Spectrum & Network Measurements* available through a VXI Technology Sales Office.

delta sigma

A method for converting an analog input to digital data. It involves using a difference of two voltages (delta) and a summation of signals (sigma) to improve accuracy.

digitizer

An instrument which converts analog signals into digital data suitable for digital signal processing.

DRAM

Dynamic Random Access Memory.

DSP
Digital Signal Processing.

DTB arbitration bus
The VT1432A does not use the arbitration bus. The arbitration bus is part of the VXI specification and is used by some modules to request bus control.

ECL
Emitter-Collector Logic, a standard for electrical signals.

Engineering Unit (EU)
A scale factor used to convert the output of a transducer (in volts) into another unit (for example: g's).

FFT
Fast Fourier Transform.

FIFO
First-In First-Out. A buffer and controller used to transmit data. The FIFO in the VT1432A/VT1433B input is implemented using DRAM.

freerun counter
A counter in which the bits always increment. When the freerun counter reaches all ones it resets to all zeros and continues counting.

Fs
Sample Frequency or sample rate.

group ID
Any number of channels may be declared and uniquely identified by a groupID. A channel can be a member of more than one group.

holdoff time
A circuit that detects a trigger signal will not respond to another trigger until the holdoff time has passed. This prevents a ringing signal from be detected as multiple triggers.

IACK
Interrupt ACKnowledge.

IRQ
Interrupt ReQuest.

kSamples/s
Kilosamples per second.

LED
Light Emitting Diode.

Local Bus
A high-speed port defined as a standard byte-wide ECL protocol which can transfer measurement data at up to 2.62 MSamples per second from left to right on the VXI backplane.

logical address
The VXI logical address identifies where each module is located in the memory map of the VXI system.

message-based VXI device
Message-based devices communicate with the VXI Bus using high-level ASCII commands. Programming is easier and more sophisticated, but communication is slower than with register-based devices. Message-based devices can also be programmed at the register level. The VT1432A and VT1433B are register-based VXI devices.

module-dependent commands
Commands that are module-dependent change a parameter for all channels of the module; even when only one channel has been specified in the channel list.

MXI bus
A bus standard which can be used to connected multiple VXI mainframes.

overlap block mode
A mode of data-collecting in used in the VT1432A and VT1433B. It is similar to block mode except that it allows additional arms and triggers to occur before an already-acquired block is sent to the host.

pipeline mode
A Local Bus mode in which data is sent through a module and on to the next one.

Plug&Play
See VXI*plug&play*

RAM
Random Access Memory.

register-based VXI device

Register-based devices communicate with the VXI Bus by way of registers. They must be programmed with low-level binary commands but they can communicate faster than message-based devices. The VT1432A and VT1433B are register-based VXI devices.

registers

Memory locations in the hardware of a VXI module which can be used to program the module at a low level.

RPM

Revolutions Per Minute.

ROM

Read-Only Memory

SCA

Signal Conditioning Assembly. An example is the 4-channel input assemblies used in the VT1432A (also called Vibrato).

sample rate

The rate at which the measurement data is sampled. For the VT1432A, the sample rate is 2.56 times the frequency span. Sample rate is abbreviated “Fs” (for “sample Frequency”).

settling

When settling, the digital filter waits a designated number samples before outputting any data.

SFP

see Soft Front Panel

shared memory

Memory locations in both a VXI module and in a host or controller which are shared and can be used to transmit data between the host and module.

slot 0 commander

The module which occupies the left-most slot in a VXI mainframe. It supplies important signals for the rest of the system.

SMB

Sub-Miniature “B”; a type of connector.

Soft Front Panel (SFP)
A VXI*plug&play* program which provides and easy-to-use interface for the VT1432A. It can be used in Microsoft Windows 95 or later or Windows NT.

SRAM
Static Random Access Memory.

summer
A circuit that outputs the sum of two input signals.

sync/trigger line
A TTL line on the VXI back plane, used for synchronization or triggering signals.

SYSRESET*
SYStem RESET line, part of the VXI Bus.

system module
The module with the lowest VXI logical address. It needs to be set to output the synchronization pulse for a multiple module group. All system sync pulses come from the system module.

tachometer
The tachometer produces a signal which is proportional to the rotation of a device. It can be programmed to produce one or more signals per revolution.

target
The ‘target’ of a library function is either a channel, a group or (rarely) a module, depending on the nature of the call. When the same library function may be called with either a channel or a group identifier, its ‘target’ is shown by a parameter named ID.

TTL
Transistor-Transistor Logic, a standard for electrical signals.

TTLTRG
TTL TRiGger lines, part of the VXI Bus.

VEE
Virtual Engineering Environment, a program which facilitates the setup and programming of instruments by employing a graphic user interface.

VME Bus
An industry-standard bus on the VXI backplane for module control, setup and measurement data transfers. For measurement data transfers, the Local Bus offers higher transfer rates.

VXI

VME Extensions for Instrumentation, a standard specification for instrument systems.

VXI*plug&play*

A set of standards which provides VXI users with a level of standardization across different vendors beyond what the VXI standard specifications spell out.

zoom

In instruments that support zoom a frequency span can be selected around a specified center frequency to allow a specific frequency band to be focused on.

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Declaration of Conformity

According to ISO/IEC Guide 22 and EN 45014

Manufacturer's name:	VXI Technology, Inc.
Manufacturer's address:	VXI Technology, Inc. 2031 Main Street Irvine, CA 92614-6509

declares, that the product

Product Name:	4-Channel, 65 kSamples/s, Arbitrary Source
Model Number:	VT1434A

conforms to the following specifications:

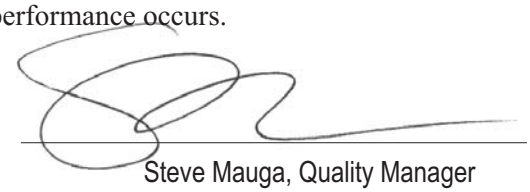
Safety:	IEC 1010-1:1990+A1/EN61010:1993
EMC:	CISPR 11: 1990/EN55011 (1991), Group1, Class A EN50082-1 IEC 801-2: 1991/EN50082-1 (1992): 4 kV CD, 8 kV AD IEC 801-3: 1984/EN50082-1 (1992): 3 V/m (1) IEC 801-4: 1988/EN50082-1 (1992): 1 kV

Supplementary Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC.

(1) In a 3 V/m field, some degradation of product performance occurs.

Irvine, CA - July 30, 2004



Steve Mauga, Quality Manager